17A, 600kHz, 20V Wide Input Range,

Synchronous Boost Converter

CE8451 Series

■ INTRODUCTION

The CE8451 is a 600kHz fixed-frequency, high-efficiency, wide input range, current-mode boost converter with optional internal or external current-sensing configuration for high-integration and high-power applications. With a current limit above 17A, the CE8451 supports a wide range of applications including POS, Thunderbolt, Bluetooth Audio, Power Banks, and Fuel Cells. The CE8451 features a 10mΩ, 24V power switch and a synchronous gate driver for high efficiency. An external compensation pin gives the user flexibility in setting loop dynamics and obtaining optimal transient performance at all conditions.

The CE8451 includes under-voltage lockout (UVLO), switching-current limiting and thermal shutdown (TSD) to prevent damage in the event of an output overload.

The CE8451 is available in a low-profile 22-pin 3mmx4mm QFN package.

■ FEATURES

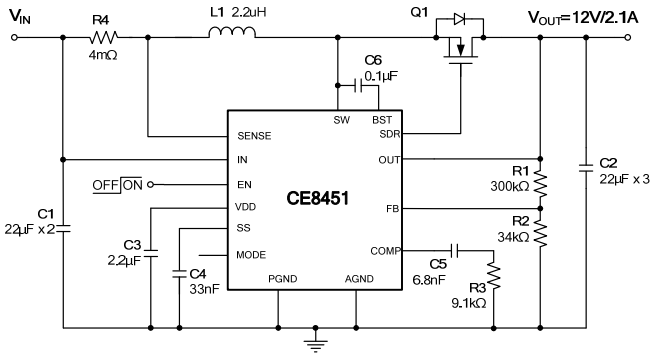
- 3V-to-20V Wide Input Range
- Integrated 10mΩ Low-Side Power FET
- SDR Driver for Synchronous Solution
- >17A Switch-Current Limit
- Up to 97.5% Efficiency
- Optional Internal/External Current-Sensing Configuration
- External Soft-Start and Compensation for Higher Flexibility
- Programmable UVLO and Hysteresis
- < 1μA Shutdown Current
- Thermal Shutdown at 150℃
- Available in a 3x4mm QFN-22 Package

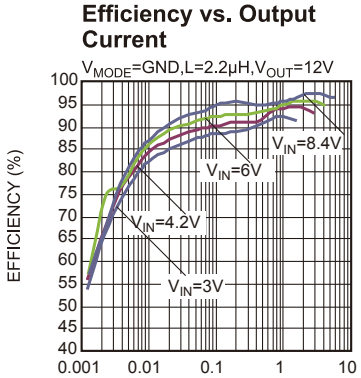
■ APPLICATIONS

- Thunderbolt Interface
- Notebooks and Tablets
- Bluetooth Audio
- Power Banks
- Fuel Cells
- POS Systems

All CHIPOWER parts are lead-free and adhere to the RoHS directive.

■ TYPICAL APPLICATION





■ ORDERING INFORMATION

Part Number*	Package
CE8451AQD10	QFN-22 (3mm×4mm)

■ PIN CONFIGURATION

TOP VIEW

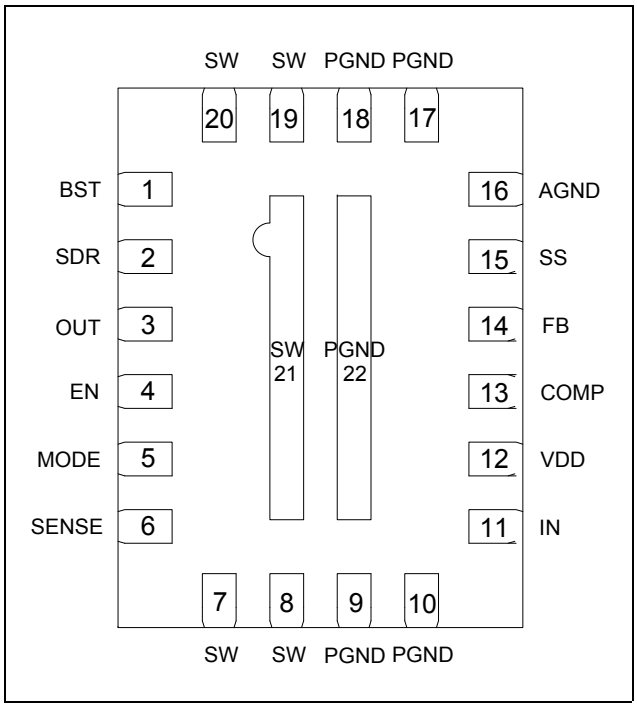


Table 1. Pin Functions

Pin NO.	Name	Description
1	BST	Bootstrap. BST powers the SDR driver.
2	SDR	Synchronous Gate Driver for the Output Rectifier.
3	OUT	Sample Output Voltage. OUT provides the sample output voltage and the charge for the BST capacitor. VDD is powered from OUT when V_{OUT} is higher than V_{IN}.
4	EN	Chip Enable Control Input. Active high. Regulator on/off control input. When not used, connect EN to the input source through a 100kΩ pull-up resistor for automatic start-up (if V_{IN} > 5.5V). Also, EN can program Vin UVLO. Do not leave EN floating.
5	MODE	Mode Select. Selects the internal or external current sensing mode. Connect to GND to use internal current-sensing block. If floating, use an external current-sense resistor. DO NOT pull MODE down to GND through a resistor.
6	SENSE	Voltage Sense. Voltage sensed between SENSE and IN. The voltage sensed between SENSE and IN determines the external current-sense signal.
7,8,19,20,21	SW	Power Switch Output. SW is the drain of the internal Power MOSFET. Connect the power inductor and output rectifier to SW.
9,10,17,18,22	PGND	Power Ground.
11	IN	Input Supply. IN must be bypassed locally.
12	VDD	Internal Bias Supply. Decouple with a 2.2μF ceramic capacitor as close to FB as possible.
13	COMP	Compensation. Connect a capacitor and resistor in series to AGND for loop stability.
14	FB	Feedback Input. Reference voltage is 1.225V. Connect a resistor divider from V_{OUT} to FB.
15	SS	Soft-Start Control. Connect a soft-start capacitor to SS. The soft-start capacitor is charged with a constant current. Leave SS disconnected if the soft-start is not used.
16	AGND	Analog Ground.

■ ABSOLUTE MAXIMUM RATINGS (1)

SW .....–0.3V to +24V (28V for <10ns)
IN, SENSE, OUT .....–0.3V to +24V
MODE .....–0.3V to Vin+5.5V
BST, SDR .....–0.3V to Vsw+5.5V
All Other Pins.....–0.3V to +5.5V
EN bias current..... 0.5mA(2)
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C
Continuous Power Dissipation (T_A= +25°C)(3)
..... 2.6W

■ *RECOMMENDED OPERATING CONDITIONS* (4)

Supply Voltage V_{IN} .....3V to 20V
Output Voltage V_{OUT}.....V_{IN} to 22V
EN bias current.....0mA to 0.3mA(2)
Operating Junction Temp.(T_J).. -40°C to +125°C

■ *Thermal Resistance* (5)

		θ_{JA}	θ_{JC}	
QFN-22 (3mmx4mm)	….	48	11	°C/W

Notes:

1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommend -ed operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
2) Refer to “Enable and Programmable UVLO” section
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

■ ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to 125°C, typical value is tested at 25°C, unless otherwise noted.

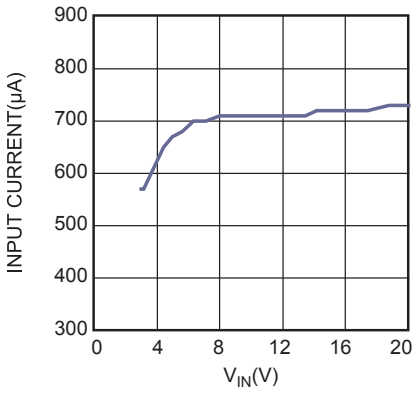
Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		3		20	V
Input UVLO	IN_{UVLO-R}	V_{IN} Rising	2.6	2.68	2.76	V
Input UVLO Hysteresis	$IN_{UVLO-HYS}$			250		mV
Operating VDD Voltage	V_{DD}	V_{IN}=12V		5		V
Shutdown Current	I_{SD}	V_{EN} = 0V, Measured on IN pin, T_J=25°C			1	μA
Quiescent Current	I_Q	V_{FB} = 1.35V, Measured on IN pin		600	750	μA
Switching Frequency	F_S	T_J=25°C	510	600	690	kHz
		T_J=-40°C to 125°C	450		690	
Minimum Off Time	$T_{MIN-OFF}$	V_{FB} = 0V		220		ns
Minimum On Time (7)	T_{MIN-ON}			120		ns
EN Turn-On Threshold	V_{EN-ON}	V_{EN} Rising (switching)	1.27	1.33	1.39	V
EN High Threshold	V_{EN-H}	V_{EN} Rising (micro power)			1.0	V
EN Low Threshold	V_{EN-L}	V_{EN} Falling (micro power)	0.4			V
EN Turn-On Hysteresis Current	I_{EN-HYS}	1.0V < EN < 1.4V	3	4.5	6	μA
EN Input Bias Current	I_{EN}	V_{EN} = 0V, 3.3V		0		μA
Soft-Start Charge Current	I_{SS}		5	7	9	μA
FB Reference Voltage	V_{FB}	T_J=25°C	1.212	1.225	1.238	V
		T_J=-40°C to 125°C	1.207	1.225	1.243	
FB Input Bias Current	I_{FB}	V_{FB}=1V	–50			nA
SDR Rise Time(7)	T_{SDR_Rise}	C_{Load}=2.7nF, Test from 10% to 90%		20		ns
SDR Fall Time(7)	T_{SDR_Fall}	C_{Load}=2.7nF, Test from 90% to 10%		30		ns
Error Amp Voltage Gain(6)	A_{V_EA}			300		V/V
Error Amp Transconductance	G_{EA}			160		μA/V
Error Amp Max Output Current		V_{FB}=1V or 1.5V		22		μA
Current to COMP Gain	Gcs	V_{MODE}=GND		27		A/V
Sense to COMP Gain	Gxcs	MODE pin float, $\Delta V_{SENSE}/\Delta V_{COMP}$		103		mV/V
Comp Threshold for Switching (7)	V_{PSM}			0.5		V
Comp High Clamp				1.8		V
SW On Resistance	R_{ON}			10		mΩ
SW Current Limit	I_{LIMT}	V_{MODE}=GND, Duty Cycle = 40%, T_J=25°C	17	22		A
External Sense Average-Current Limit	V_{CL}	MODE pin float	45	54	63	mV
External Sense-Current Limit Protection Time	T_{CL}	MODE pin float		1.1		ms
Thermal Shutdown(7)	T_{SD}			150		°C
Thermal Shutdown Hysteresis(7)	T_{SD-HYS}			25		°C

Notes:
6) Guaranteed by Design.
7) Guaranteed by engineering sample Characterization, not tested in production.

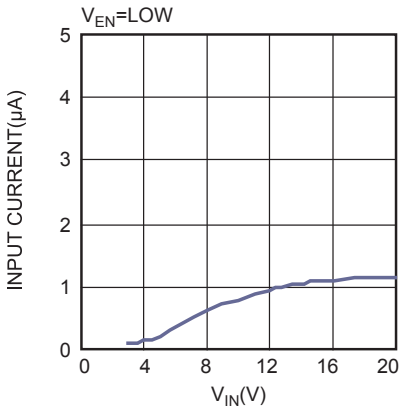
■ TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 2.2μH, T_A = 25°C, unless otherwise noted.

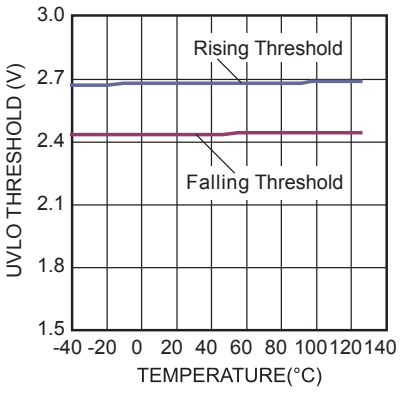
Quiescent Current vs. Input Voltage



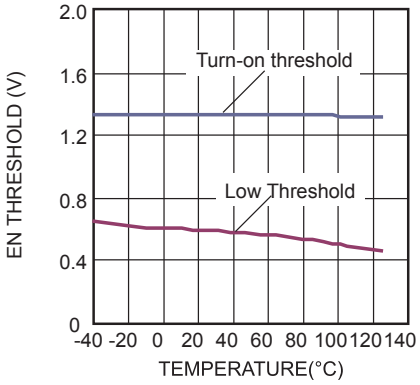
Shutdown Current vs. Input Voltage



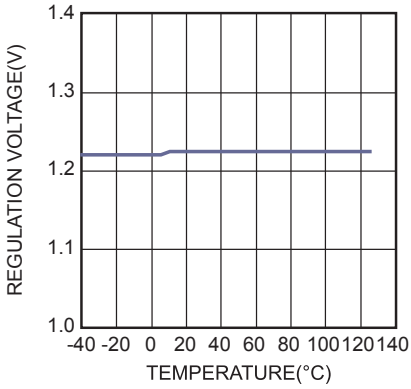
V_{IN} UVLO Threshold vs. Temperature



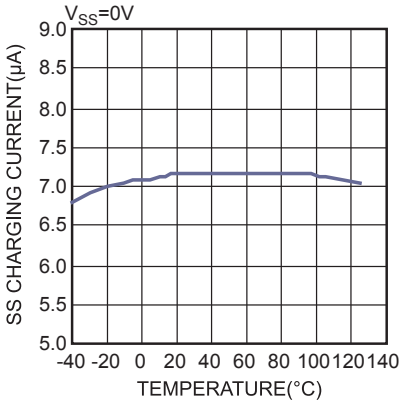
EN Threshold vs. Temperature



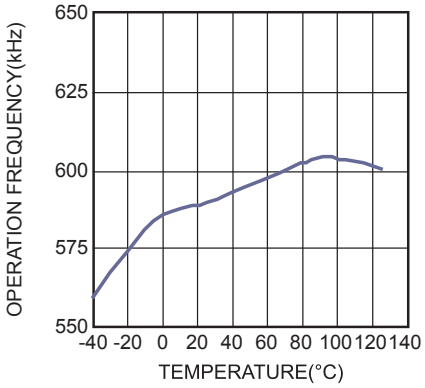
V_{REF} vs. Temperature



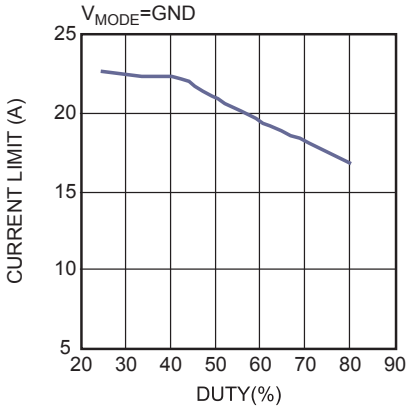
SS Charge Current vs. Temperature



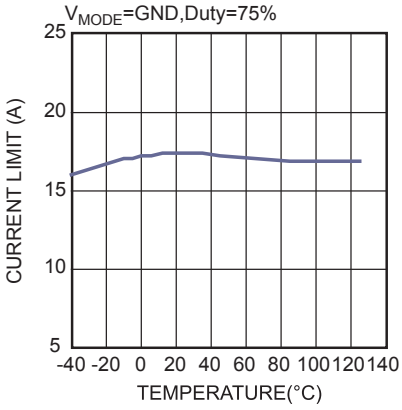
Switch Frequency vs. Temperature



Current Limit vs. Duty Cycle



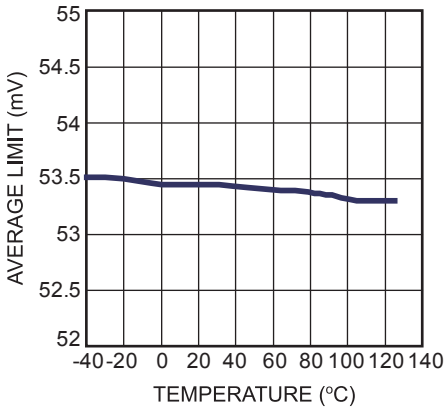
Current Limit vs. Temperature



■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 2.2μH, T_A = 25°C, unless otherwise noted.

External Sense Average-Current Limit vs. Temperature

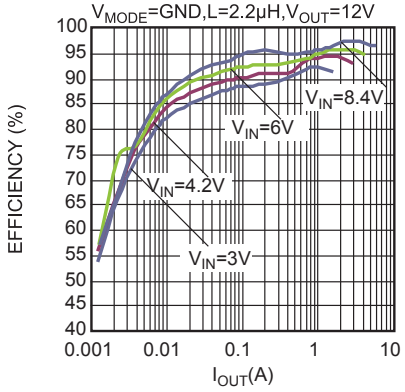


■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3V, V_{OUT} = 12V, L = 2.2μH, I_{OUT}=2A, C_{OUT}=22μF*3, V_{MODE}=float, R_{SENSE}=4mΩ T_A = 25°C, unless otherwise noted.

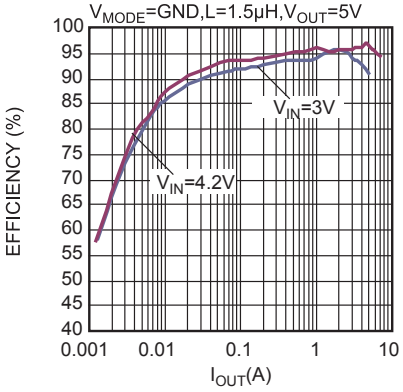
Efficiency vs. Output Current

V_{MODE}=GND,L=2.2μH,V_{OUT}=12V



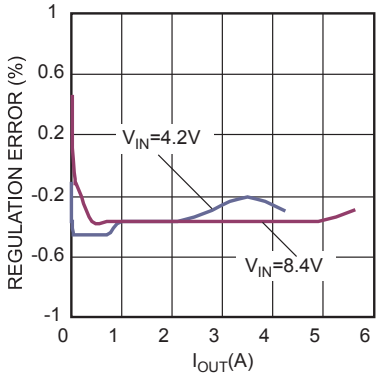
Efficiency vs. Output Current

V_{MODE}=GND,L=1.5μH,V_{OUT}=5V



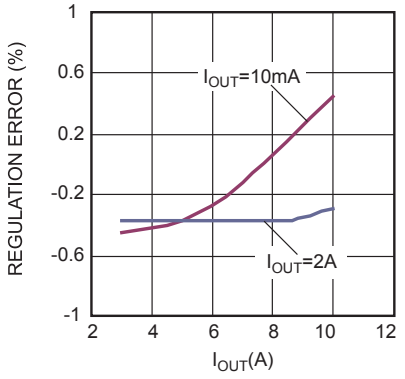
Load Regulation

V_{MODE}=GND



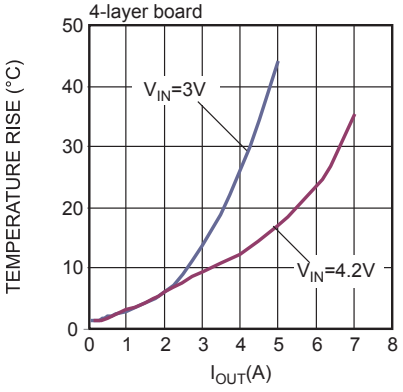
Line Regulation

V_{MODE}=GND



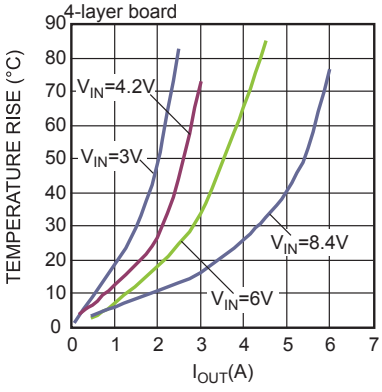
Case Temperature Rise vs. Output Current

V_{MODE}=GND, V_{OUT}=5V,
4-layer board



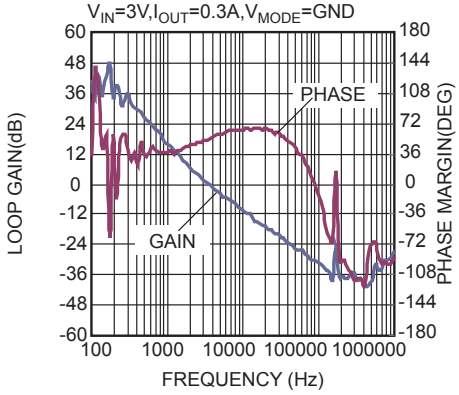
Case Temperature Rise vs. Output Current

V_{MODE}=GND, V_{OUT}=12V,
4-layer board



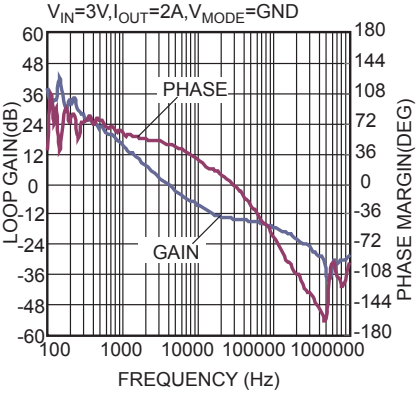
Bode Plot

V_{IN}=3V,I_{OUT}=0.3A,V_{MODE}=GND



Bode Plot

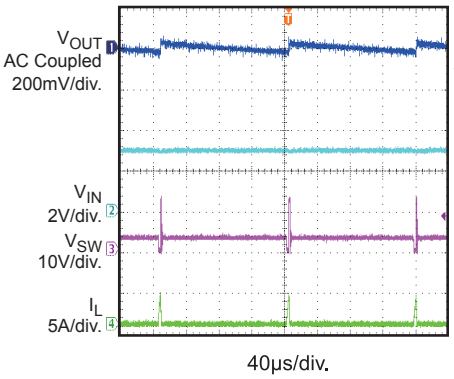
V_{IN}=3V,I_{OUT}=2A,V_{MODE}=GND



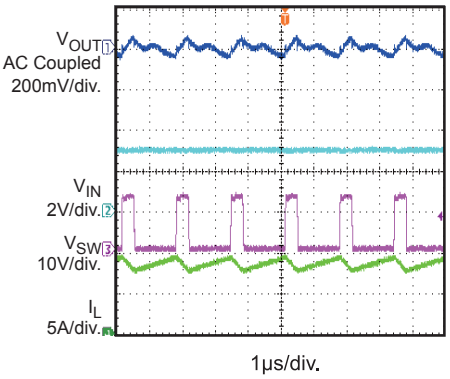
■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3V, V_{OUT} = 12V, L = 2.2μH, I_{OUT}=2A, C_{OUT}=22μF*3, V_{MODE}=float, R_{SENSE}=4mΩ T_A = 25°C, unless otherwise noted.

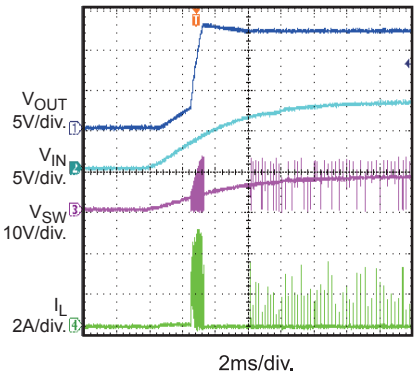
Steady State
I_{OUT}=0.01A



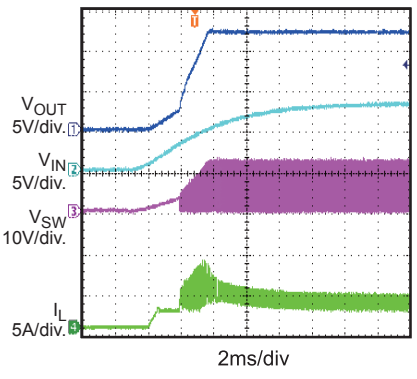
Steady State
I_{OUT}=2A



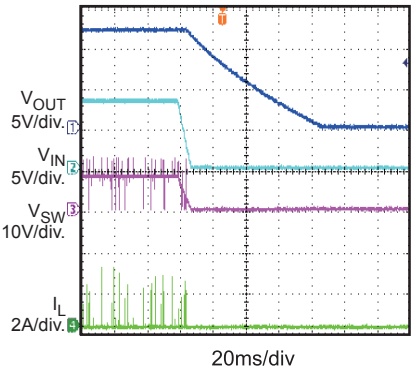
V_{IN} Start-Up
V_{IN}=8.4V, I_{OUT}=0.01A



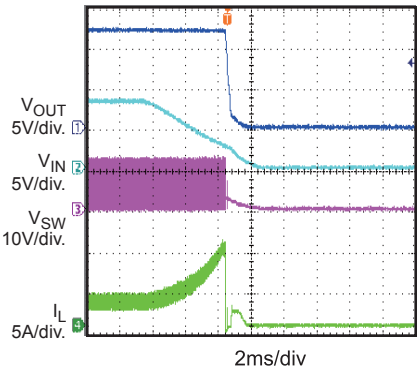
V_{IN} Start-Up
V_{IN}=8.4V, I_{OUT}=2A



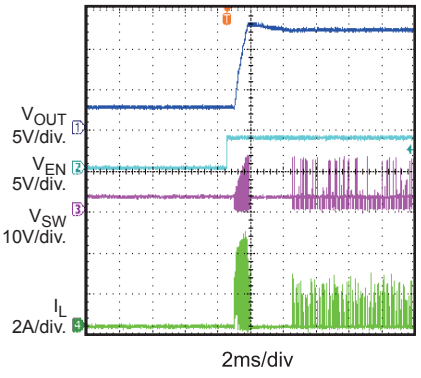
V_{IN} Shutdown
V_{IN}=8.4V, I_{OUT}=0.01A



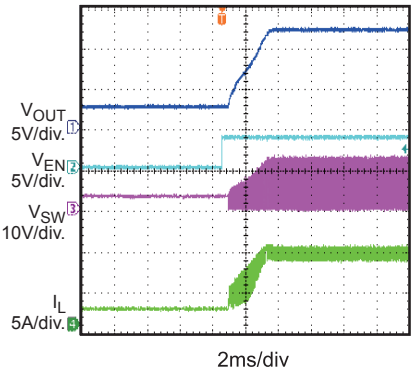
V_{IN} Shutdown
V_{IN}=8.4V, I_{OUT}=2A



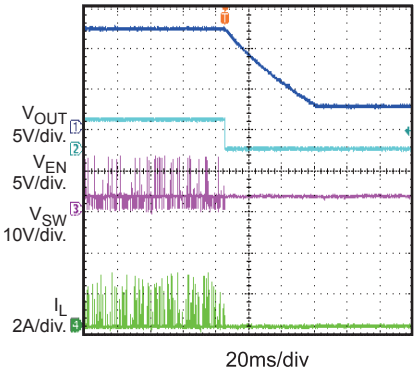
EN Start-Up
I_{OUT}=0.01A



EN Start-Up
I_{OUT}=2A



EN Shutdown
I_{OUT}=0.01A

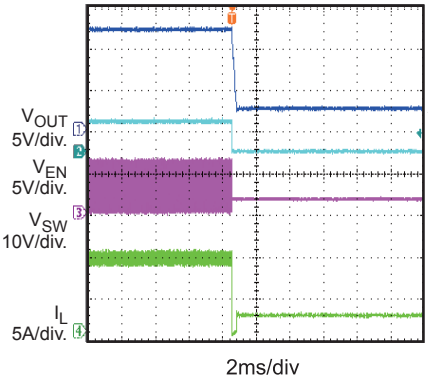


■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3V, V_{OUT} = 12V, L = 2.2μH, I_{OUT}=2A, C_{OUT}=22μF*3, V_{MODE}=float, R_{SENSE}=4mΩ T_A = 25°C, unless otherwise noted.

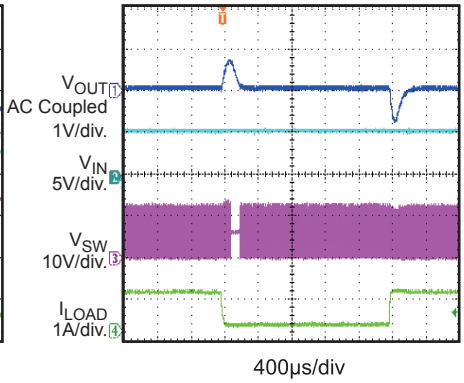
EN Shutdown

I_{OUT}=2A



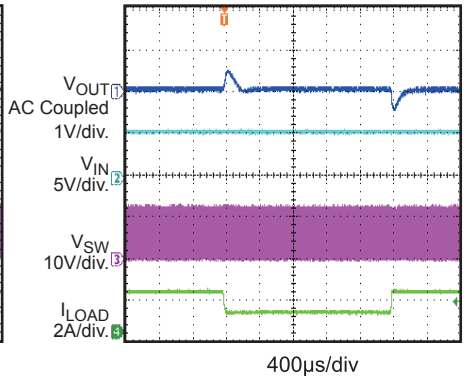
Load Transient

V_{IN}=6V, I_{OUT}=0.2-1A@25mA/μs



Load Transient

V_{IN}=6V, I_{OUT}=1-2A@25mA/μs



■ FUNCTIONAL BLOCK DIAGRAM

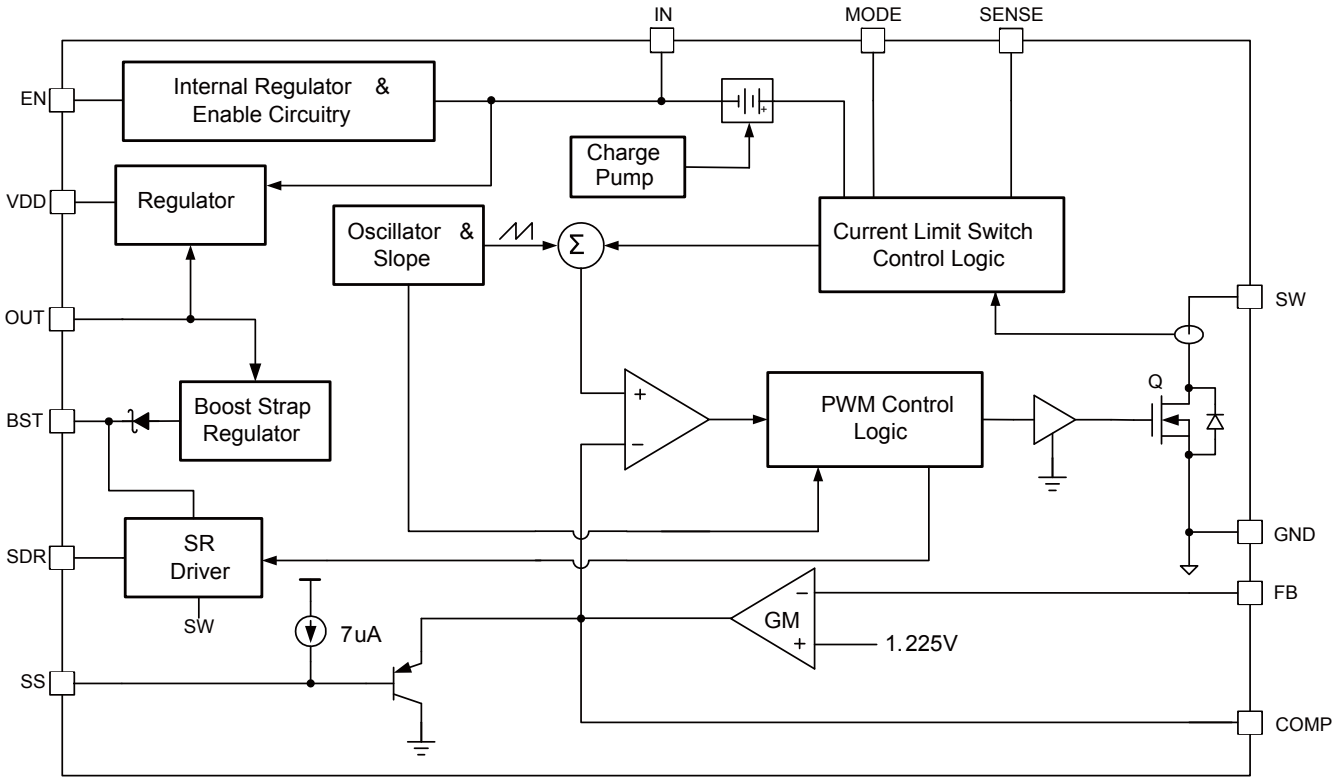


Figure 1. Functional Block Diagram

■ OPERATION

The CE8451 is a 600kHz fixed-frequency, high-efficiency, wide input range, current-mode boost converter with optional internal or external current-sensing configuration for high-integration and high-power applications (see Figure 1).

Boost Function

The CE8451 uses constant frequency, peak-current mode, boost regulation architecture to regulate the feedback voltage.

At the beginning of each cycle, the N-channel MOSFET switch Q is turned on, forcing the inductor current to rise. When floating MODE, the current at the source of switch Q is measured externally; then it is converted to a voltage by the current-sense amplifier. That voltage is compared to the error voltage on COMP (which is an amplified version of the difference between the 1.225V reference voltage and the feedback voltage). When these two voltages are equal, the PWM comparator turns off switch Q. This forces the inductor current into the output capacitor through the external rectifier, causing the inductor current to decrease. The peak-inductor current is controlled by the voltage on COMP, which in turn is controlled by the output voltage. To satisfy the load, the output voltage is regulated by the inductor current. Current mode regulation improves transient response and control loop stability.

VDD Power

CE8451 is powered by VDD. A ceramic capacitor no less than 2.2μF is required to decouple VDD. During start-up, VDD power is regulated by IN. Once the output voltage exceeds the input voltage, VDD is powered from V_{OUT} (instead of V_{IN}). This allows the CE8451 to maintain low R_{ON} and high efficiency, even with low-input voltage.

Soft-Start (SS)

CE8451 uses one external capacitor on SS to control SW frequency during start-up. The operation frequency is initially 1/4 of the normal frequency. As the SS capacitor is charged, the frequency increases continuously. When the voltage on SS exceeds ~0.65V, the frequency switches to a normal frequency. In addition, the voltage on COMP is clamped within V_{SS}+0.7V. During start-up the COMP voltage reaches 0.7V quickly, and then rises at the same rate of V_{SS}. These two mechanisms prevent high-inrush current from the input power supply.

SDR and BST Function

The CE8451 generates a synchronous gate-driving signal that complements the gate driver of the internal MOSFET. The SDR driver is powered from BST (5V, typically) and a low Q_G N-channel MOSFET (a gate-source threshold voltage lower than 3V is preferred). In high-power applications, using a synchronous rectifier switch improves overall conversion efficiency. If a synchronous rectifier switch is not used, float SDR.

The 5V driver power-bootstrap voltage is powered from OUT. If output voltage is low (or the duty cycle is too low), BST voltage may not be regulated to 5V, triggering a BST_UVLO. A schottky diode from an external 5V source to BST is recommended, otherwise, the SDR driver signal may be lost.

Current Sensing Configuration

The CE8451 offers the option of using the internal circuit or an external resistor to sample the inductor current. When using the internal current sense, MODE must be connected directly to GND before powering on. Meanwhile, SENSE should be connected to IN. In this configuration, sensed current is compared to both the COMP voltage and the limit peak current cycle-by-cycle during an overload condition.

When floating MODE, the inductor current is sampled by an external sense resistor between IN and SENSE. Under this configuration, sensed current is compared with COMP for low-side switch on/off control. However, the overload is protected by the average inductor current. When the sensed current signal exceeds 54mV, COMP is pulled low to regulate the boosted current. This causes the CE8451 to enter hiccup mode (after 1.1ms). The CE8451 re-starts after about 60ms in hiccup mode.

If the sampled current signal rises to 100mV (within the 1.1ms blank time), immediately the CE8451 operates in hiccup mode.

The CE8451 starts switching in internal current-sense mode after it detects 0V on MODE. In external current-sense mode, CE8451 detects MODE voltage and starts switching (after MODE is higher than Vin + 2V). In over-current or hiccup mode, MODE is pulled low. If the average current limit is triggered before switching, CE8451 may not start switching because MODE is regulated to low in an overload condition.

If the peak-inductor current is higher than 6A, an external current-sensing resistor is recommended. Do NOT change the sensing configuration when CE8451 is in operation.

Light-Load Operation

To optimize efficiency at light load, CE8451 employs a pulse-skipping mechanism and foldback frequency. When the load becomes lighter, the COMP voltage decreases, causing the CE8451 to enter foldback operation (the lighter the load, the lower the frequency). However, if the load becomes exceedingly low, CE8451 enters PSM. PSM operation is optimized so that only one SW pulse is launched every burst cycle; therefore the output ripple is very low.

Enable (EN) and Programmable UVLO

EN enables and disables the CE8451. When applying voltage higher than the EN higher threshold (1V, typically), CE8451 starts up some of the internal circuits (micro-power mode). If EN voltage exceeds the turn-on threshold (1.33V), the CE8451 enables all functions and starts boost operation. Boost operation is disabled when EN voltage falls below its lower threshold (1.33V). To completely shut down the CE8451, <0.4V low-level voltage is required on EN. After shutdown, CE8451 sinks a current from input power (less than 1uA, typically).

The maximum recommended voltage on EN is 5.5V. If the EN control signal comes from a voltage higher than 5.5V, a resistor should be added between EN and the control source. An internal Zener diode on EN clamps the EN voltage to prevent runaway. Ensure the Zener clamped current flowing into EN is less than 0.3mA.

Meanwhile, EN can program Vin's UVLO (see "Applications\UVLO Hysteresis" section).

Thermal Shutdown (TSD)

To prevent thermal damage, the device has an internal temperature monitor. If the die temperature exceeds 150°C, the converter shuts down. Once the temperature drops below 125°C, the power supply resumes operation

■ APPLICATION INFORMATION

Selecting Current Limit Resistor

When an external resistor is used, CE8451 has an average current limit. The resistor R_{SENSE} (connected from the input voltage to SENSE), sets the current limit (I_{CL}):

$$I_{CL} = V_{CL} / R_{SENSE}$$

Where, V_{CL} is 54mV, typically, I_{CL} is in amperes, and R_{SENSE} is in mΩ.

UVLO Hysteresis

The CE8451 features a programmable UVLO hysteresis. When powering up, EN sinks a 4.5μA current from an upper resistor, R_{TOP} (see Figure 2). VIN voltage must increase to overcome the current sink. The VIN start-up threshold is determined by:

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 4.5\mu A \times R_{TOP}$$

Where, V_{EN-ON} is the EN voltage turn-on threshold (1.33V, typically).
Once the EN voltage reaches V_{EN-ON}, the 4.5uA sink current turns off to create a reverse hysteresis for the VIN falling threshold:

$$V_{IN-UVLO-HYS} = 4.5\mu A \times R_{TOP}$$

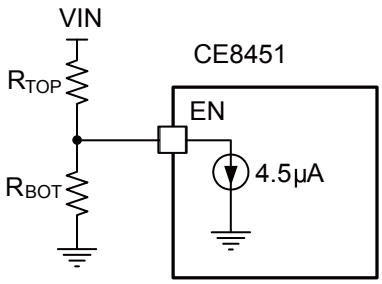


Figure 2: V_{IN} VULO Program

Selecting the Soft-Start Capacitor

To prevent excessive input current, the CE8451 includes a soft-start circuit that limits the voltage on COMP during start-up This prevents premature termination of the source voltage at start-up due to input-current overshoot. When power is applied to the device, enable is asserted and a 7μA internal-current source charges the external capacitor at SS. The SS voltage clamps COMP voltage (as well as the inductor peak current) until output is close to regulation or COMP reaches 1.8V. For most applications, a 33nF SS capacitor is sufficient.

Setting the Output Voltage

Output voltage is fed back through two sense resistors in series. The feedback reference voltage is 1.225V, typically. The equation for the output voltage is:

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2})$$

Where, R1 is the top feedback resistor, R2 is the bottom feedback resistor, and V_{REF} is the reference voltage (1.225V, typically).

Choose feedback resistors in the 10kΩ range (or higher) for good efficiency.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low ESR capacitor is required to minimize noise. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors suffice.
Two 22uF capacitors are recommended for high-power applications. The capacitor can be electrolytic, tantalum, or ceramic. However, since the capacitor absorbs the input-switching current, it requires an adequate ripple-current rating. Use a capacitor with a RMS current rating greater than the inductor-ripple current (see “Selecting the Inductor” to determine the inductor-ripple current).

To ensure stable operation, place the input capacitor as close to the IC as possible. Alternately, a smaller, high-quality ceramic 0.1μF capacitor may be placed closer to the IC with the larger capacitor placed a little farther away. When using this technique, a larger electrolytic or tantalum type capacitor is recommended. All ceramic capacitors should be placed very close to the input.

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to minimize the output-voltage ripple. The characteristics of the output capacitor affect the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. If using ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and the output-voltage ripple is independent primarily of the ESR. The output-voltage ripple is estimated by:

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times F_{SW}}$$

Where V_{RIPPLE} is the output-ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, Fsw is the 600kHz fixed-switching frequency, and C_{OUT} is the capacitance of the output capacitor.

If using tantalum or low ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, so the output ripple is estimated as:

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times F_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}}$$

Where, R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor that satisfies output ripple and load transient design requirements. Take capacitance de-rating into consideration when designing high output-voltage applications. For most applications, three 22μF ceramic capacitors are suitable.

Selecting the Inductor

The inductor forces a higher output voltage while being driven by the input voltage. A higher value inductor has less ripple current, resulting in a lower peak-inductor current. This reduces stress on the internal N-channel switch and enhances efficiency. However, a higher value is physically larger, has a higher series resistance, and a lower saturation current.

A good rule of thumb is to have a peak-to-peak ripple current that is approximately 30%-40% of the maximum input current. To prevent loss of regulation due to the current limit, ensure the peak-inductor current is below 75% of the current limit at the operating duty cycle. Also, ensure that the inductor does not saturate under the worst-case load transient and start-up conditions. Calculate the required inductance value using the equation below:

$$L = \frac{V_{IN}\times(V_{OUT}-V_{IN})}{V_{OUT}\times F_{SW}\times \Delta I}$$

$$I_{IN(max)} = \frac{V_{OUT}\times I_{LOAD(MAX)}}{V_{IN}\times \eta}$$

Where , $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor-ripple current, ΔI = (30% - 40%) x $I_{IN\ (MAX)}$, and η is efficiency.

Selecting the Output Rectifier

CE8451 features a SDR gate driver. Instead of a schottky diode, an N-channel MOSFET can be used to free-wheel the inductor current when the internal MOSFET is off. The SDR gate-driver has a high voltage level (5V), so choose an N-channel MOSFET that is compatible with a 5V gate-voltage rating. The minimum high level is 3V, typically. It is recommended that the MOSFET's turn-on threshold is lower than 3V.

In applications with low outputs (such as 5V), the voltage across the BST cap may be insufficient. If this is the case, a schottky diode should be connected from the output port to BST, conducting the current into the BST capacitor when SW is low (see Figure 3).

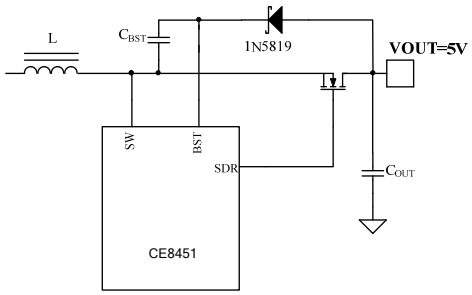


Figure 3. BST Charger for Low-Output Applications

The MOSFET voltage rating should be equal to or greater than the output voltage. The average current rating must be greater than the maximum load current. The peak-current rating must be greater than the peak-inductor current. If a Schottky diode is used as the output rectifier, the same specifications should be considered.

Compensation

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. The system uses two poles and one zero to stabilize the control loop.
The poles are F_{P1}, set by the output capacitor (C_{OUT}) and the load resistance, and F_{P2}, which starts from the origin. The zero F_{Z1} is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). These are determined by the equations:

$$F_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz)$$

$$F_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz)$$

Where, R_{LOAD} is the load resistance.
The DC loop gain is calculated as follows:

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS} \times R_{COMP}}{2 \times V^2_{OUT}} (V/V)$$

Where G_{CS} is the compensation voltage to the inductor-current gain, A_{VEA} is the error amplifier voltage gain, and the V_{FB} is the feedback regulation threshold.

Also, there is a right-half-plane zero (F_{RHPZ}) that exists in continuous conduction mode (CCM). The inductor current does not drop to zero each cycle. The frequency of the right-half plane zero is:

$$F_{RHP} = \frac{R_{LOAD}}{2 \times \pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz)$$

The right-half-plane zero increases the gain and reduces the phase simultaneously, resulting in a smaller phase and gain margin. The worst case happens during conditions of minimum input voltage and maximum output power.

Compensation recommendations are listed in the “Typical Application Circuits” section.

PCB Layout Guide

High-frequency switching regulators require very careful PCB layout for stable operation and low noise. All components must be placed as close to the IC as possible.

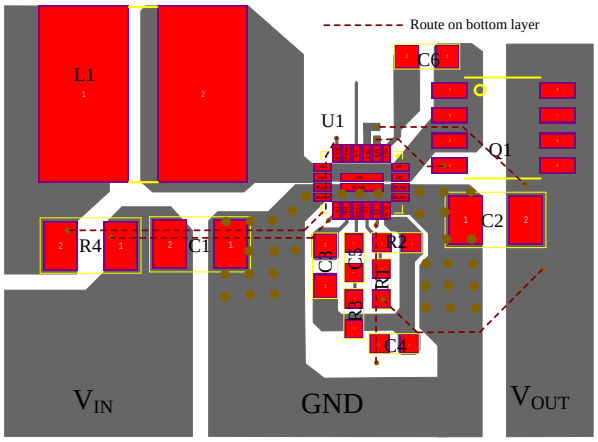


Figure 4. PCB Layout Reference

Refer to Figure 4 and the guidelines below to optimize performance:

1. Keep the output loop (SW, PGND, Q1, and C2) as small as possible.
2. Place FB divider R1 and R2 as close as possible to FB.
3. Route the sensing traces (SENSE and IN) in parallel closely with a small closed area. The 0805 package is recommended for the sensing resistor (R4) to reduce parasitic inductance.
4. Connect FB and OUT feedback from the output capacitor (C2).
5. Connect the compensation components and SS capacitor to AGND with a short loop.
6. Connect the VDD capacitor to AGND with a short loop. Do not connect to PGND net before connecting to IC-AGND.
7. Connect the compensation components and SS capacitor to AGND with a short loop.
8. The input path consisting of C1, L1, SW, PGND, BST path, and SDR path should be as short as possible.

9. Place sufficient GND vias close to the IC for good thermal dissipation.
10. Do NOT place vias into the SW net.
11. Use a 4-layer PCB for high-power applications.

Design Example

Below is a design example following the application guidelines for the specifications:

Table 1. Design Example

V_{IN}	3-10V
V_{OUT}	12V
I_{OUT}	0-2A

The detailed application schematic is shown in Figure 5. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

■ TYPICAL APPLICATION CIRCUITS

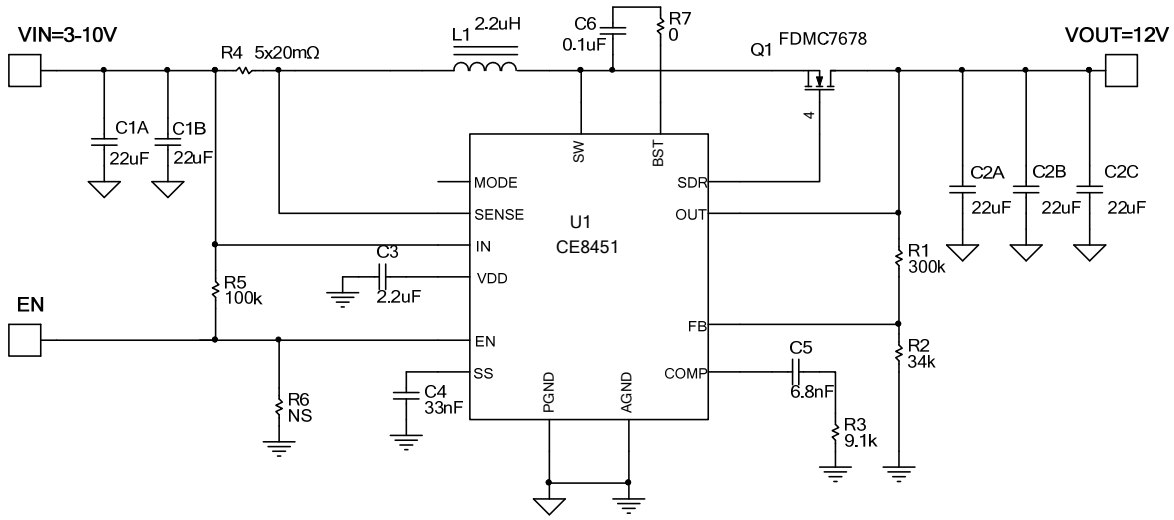


Figure 5. 12V Output Synchronous Solution Using External Current-Sensing Resistor

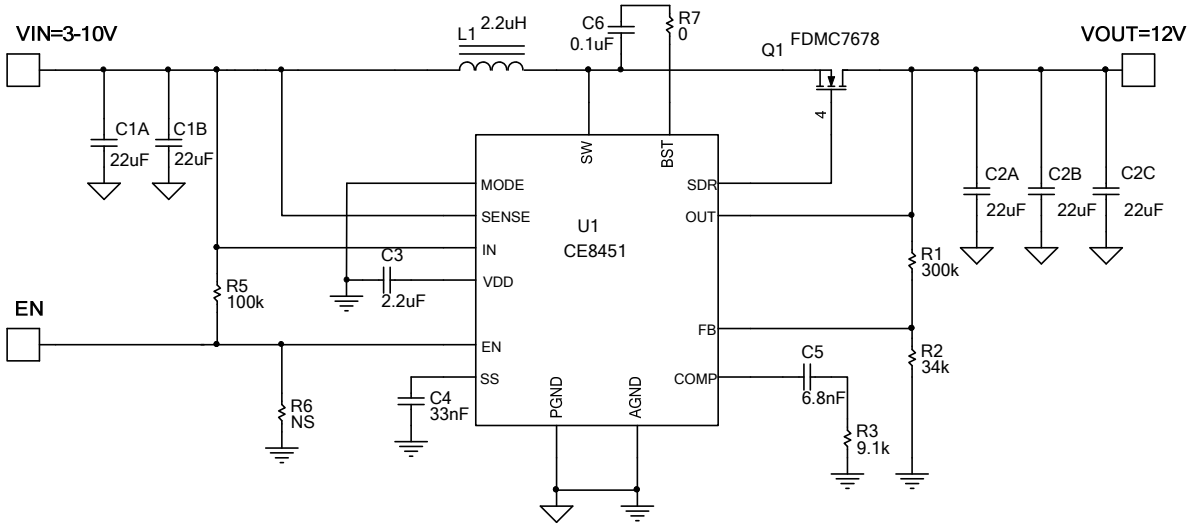


Figure 6. 12V Output Synchronous Solution Using internal Current-Sensing Circuit

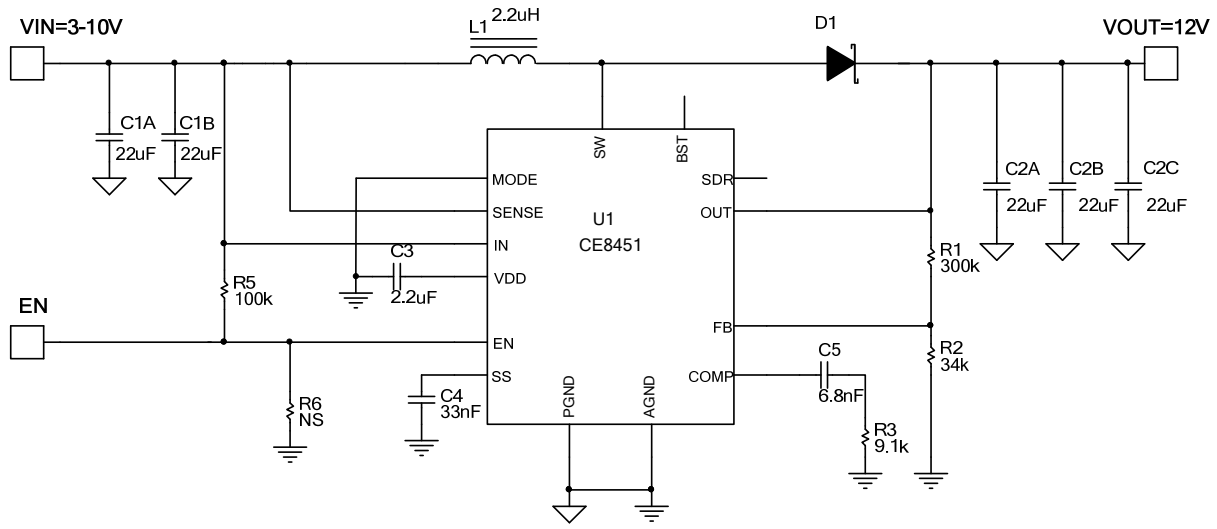


Figure 7. 12V Output Non-Synchronous Solution Using Internal Current-Sensing Circuit

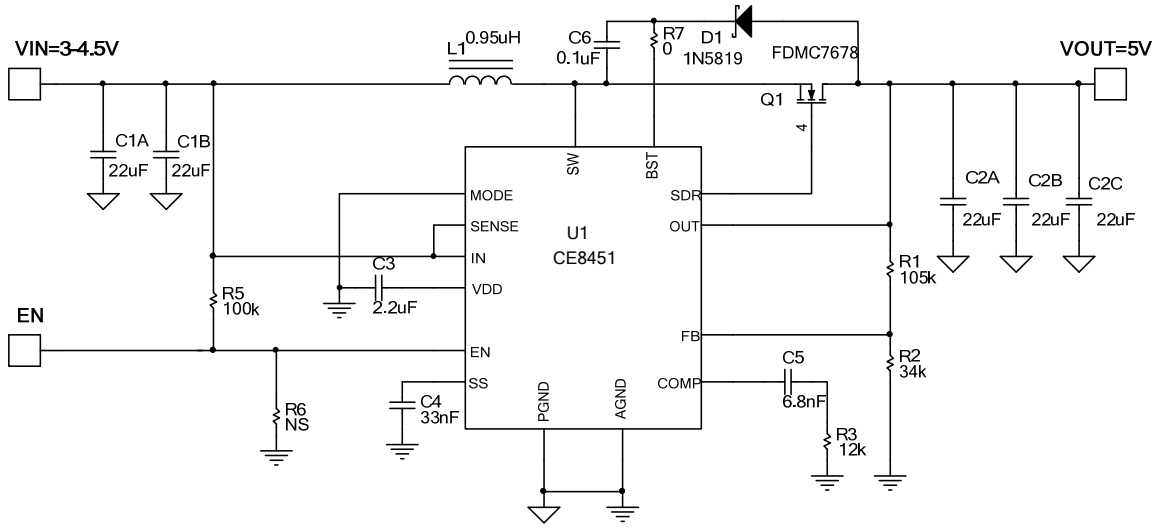
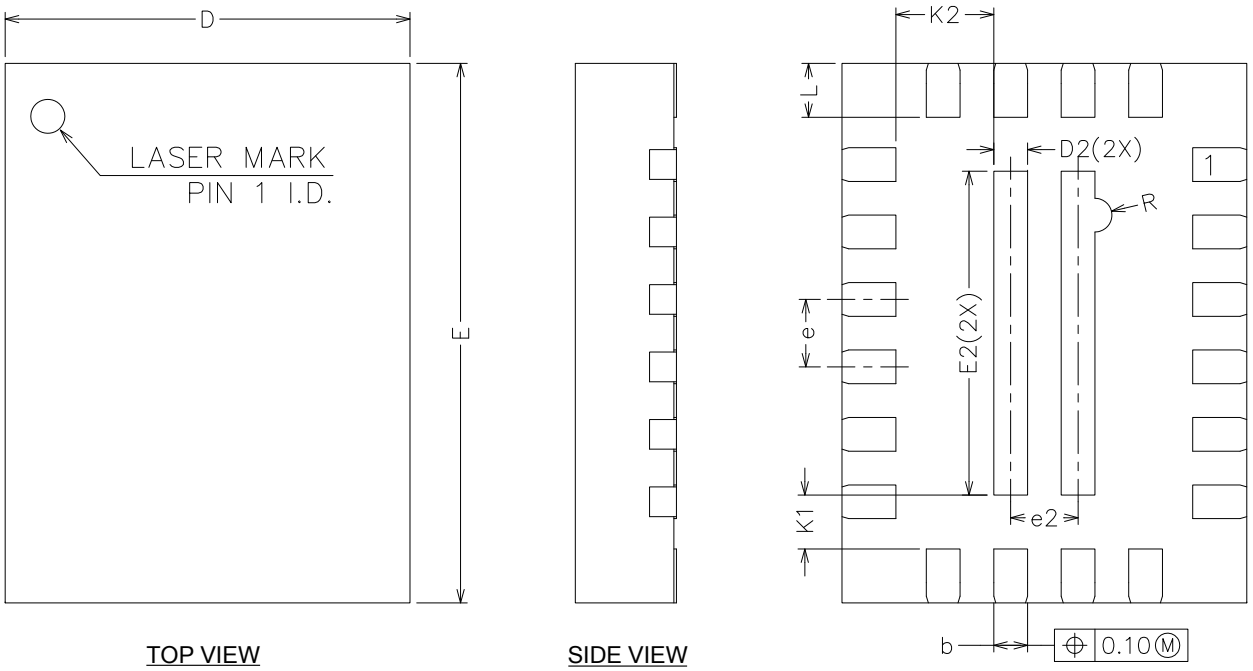


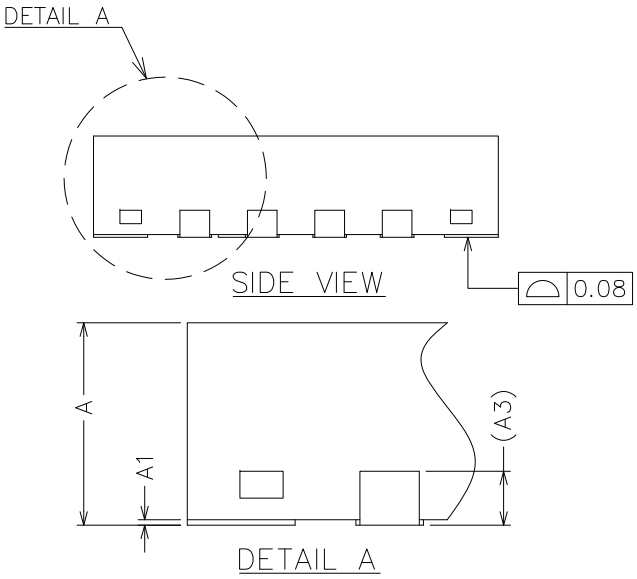
Figure 8: 5V Output Synchronous Solution Using Internal Current Sensing Circuit

■ PACKAGE INFORMATION

QFN-22 (3mmx4mm)



TOP VIEW SIDE VIEW BOTTOM VIEW



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	3.90	4.00	4.10
D2	0.15	0.25	0.35
E2	2.30	2.40	2.50
e	0.40	0.50	0.60
e2	0.40	0.50	0.60
K1	0.30	–	–
K2	0.625	–	–
L	0.35	0.40	0.45
R		0.125REF	

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.