High Efficiency 1.25MHz, 2.5A Boost Regulator **CE6373 Series**

■ INTRODUCTION:

The CE6373 is a high efficiency boost switching regulator especially designed for single cell lithium battery powered applications. It generates an output voltage of up to 5.5V from an input voltage as low as 2.7V. Ideal for applications where space is limited, it switches at 1.25MHz, allowing the use of tiny, low cost and low profile external components, minimizes solution footprint. Its internal 2.5A, 80mΩ NMOS switch provides high efficiency even at heavy load, while the constant frequency, current mode architecture results in low, predictable output noise that is easy to filter. Internal frequency compensation is designed to accommodate ceramic output capacitors, further reducing noise.

■ FEATURES:

- 1.25MHz Switching Frequency
- Built-in 80mΩ N-CH Power MOSFET Switch
- PWM/PFM Auto Switching Maintains High Efficiency Overall Load Current Range
- Up to 92% Efficiency:
  Delivers 1A@5V from Single Li Cell
- Wide Input Voltage Range: 2.7V to 6.0V
- Wide Output Voltage Range: 3.0V to 5.5V
- Output Current: 1A@V_{IN}=3.0V
- 0.6V (±2%) Feedback Reference Voltage
- Low Shutdown Current: 0.1μA(Typ.)
- Adjustable Over Current Protection:
  0.5A~2.5A
- Over Temperature Protection
- Uses Small,Low Profile External Components
- Ceramic Capacitor Compatible

■ APPLICATIONS：

- Back-up Battery
- Solar Battery Charger
- Portable Applications Using Single Li+ Cell
- Bus Powered USB Hosts
- USB Hosts Without Native 5-V Supplies
- 3G/4G Wireless Routers
- Networking card powered from PCI or PCI-express slots
- Portable Audio Players
- Personal Medical Products

■ ORDER INFORMATION

Operating free air temperature range	Output Voltage	Package	Device No.
-40~+85℃	Adjustable	SOT-23-6	CE6373CE

■ TYPICAL APPLICATION CIRCUIT

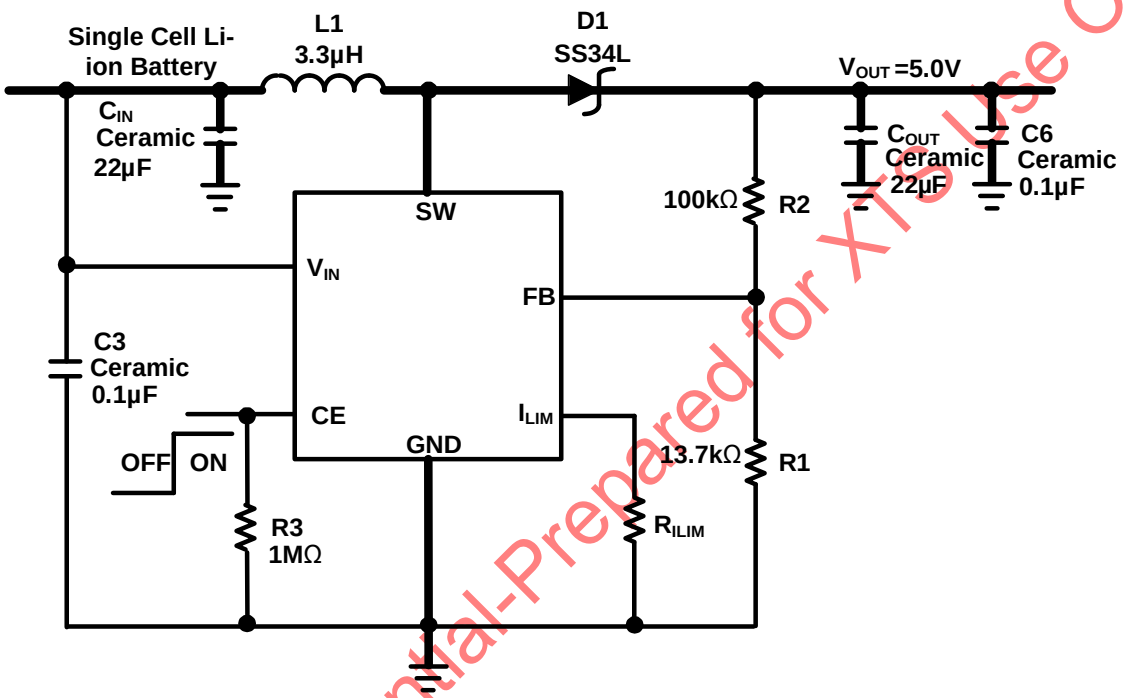
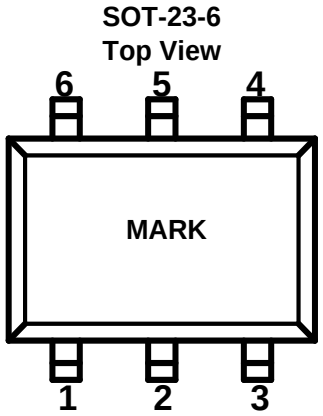


Figure 1 Standard Application Circuit

■ PIN CONFIGURATION:



SOT-23-6

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SW	I	**Switch Pin**. Connect inductor between SW and IN. A Schottky diode is connected between SW and OUT. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.
2	GND	P	**Signal and Power Ground**. Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.. This pin should be connected to a continuous PCB ground for high-current power converter as close as to the device by several vias directly under the CE6373CE for electrical contact and rated thermal performance. It dissipates the heat from the IC.
3	FB	I	**Feedback Input** Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 3.0V to 5.5V by: V_{OUT}=0.6V•[1+(R2/R1)]. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, SW、inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
4	CE	I	**Chip Enable**. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA.
5	V_{IN}	I	**Chip Supply Voltage & input Voltage Sense Input**. The V_{IN} pin should be connected to the positive terminal of the battery and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{IN} pin, and the CE6373CE GND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{IN} pin and the GND pin.
6	I_{LIM}	I	**Adjustable Input Valley Current Limit**. Can be floated for maximum current.

(1) I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, T_A=25°C)[1]

PARAMETER		SYMBOL	RATINGS	UNITS
Supply Voltage range [2]		V_{IN}	-0.3~7	V
SW Voltage[2]			-0.3~7	V
CE, FB, I_{LIM} Voltage[2]			-0.3~7	V
Peak SW Sink Current		I_{SWMAX}	2.5	A
Power Dissipation	SOT-23-6	P_d	500[3]	mW
			300[4]	mW
Operating Junction Temperature Range		T_j	-40~150	℃
Storage Temperature		T_{stg}	-40~125	℃
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	℃
ESD rating[5]		Human Body Model - (HBM)	4000	V
		Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) Surface mounted on FR-4 Board using 1 square inch pad size, dual side, 1oz copper

(4) Surface mounted on FR-4 board using minimum pad size, 1oz copper

(5) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Chipower recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

■ RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNITS
Supply voltage at V_{IN}	2.7		5.5	V
Output voltage at V_{OUT}	3.0		5.5	V
Operating free air temperature range[1], T_A	-40		85	℃
Operating junction temperature range, T_j	-40		125	℃

(1) The CE6373 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

■ ELECTRICAL CHARACTERISTICS

Typical values are at T_A=25℃, unless otherwise specified, specifications apply for condition V_{IN}=V_{CE}=3.3V, V_{OUT}=5.0V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP(1)	MAX	UNITS
SUPPLY						
Input Supply Range	V_{IN}		2.7		5.5	V
Under Voltage Lockout	V_{UVL}	V_{IN} Rising		2.2	2.7	V
UVLO Hysteresis	ΔV_{UVL}			0.2		V
Operating quiescent current into V_{IN}	I_Q	V_{FB}=0.65V, device is not switching, Measured On V_{IN},		190		μA
Average Supply Current	I_{AVG}	V_{FB}=0.55V, device is switching, Measured On V_{IN},		1.2		mA
Shutdown Current into V_{IN}	$I_{SHDNVIN}$	V_{CE}=0V		0.1	1	μA
LOGIC SIGNAL CE						
CE High-level Voltage	V_{CEH}	V_{CE} Falling, Device ON	1.5		V_{IN}	V
CE Low-level Voltage	V_{CEL}	V_{CE} Rising, Device Off			0.4	V
CE Leakage Current	I_{CE}	V_{CE}=5.0V		±0.1	±1	μA
OSCILLATOR						
Oscillator Frequency	f_{osc}		1.00	1.25	1.50	MHz
Frequency Change with Input Voltage	$\Delta f_{osc}/\Delta V_{IN}$	V_{IN}=2.7V to 5.5V		2.5		%/V
Max Duty Cycle	D_{MAX}	V_{FB}=0.55V	85	90		%
POWER SWITCH						
N-CH MOSFET On Resistance(2)	$R_{DS(ON)}$			80		mΩ
N-CH MOSFET Switch Leakage	I_{SWLEAK}	V_{CE}=0V,V_{SW}=5.0V		±0.01	±1	μA
NMOS Programmable Valley Cycle by Cycle Switch Current Limit(3)	$I_{V(CL)}$	I_{LIM} pin Floating		2.5		A
		With External Resistor: 19kΩ~96kΩ	0.5		2.5	A
Current Limit Delay to Output(4)				40		nS
OUTPUT						
Output Voltage Range	V_{OUT}		3.0		5.5	V
Feedback regulation voltage	V_{FB}		0.588	0.600	0.612	V
Line Regulation		V_{IN}=2.7V to 5.5V		0.2		%/V
Load Regulation		I_{LOAD}=0A to 1A		0.5		%/A
Feedback Input bias Current(5)	I_{FB}	V_{FB}=0.65V			0.1	μA
OVER TEMPERATURE PROTECTION						
Thermal Shutdown	T_{TSD}			150		℃
Thermal Shutdown Hysteresis	T_{TSDHYS}			30		℃

(1) Typical numbers are at 25°C and represent the most likely norm.

(2) Does not include the bond wires. Measured directly at the die.

(3) Duty cycle affects current limit due to ramp generator

(4) Specification is guaranteed by design and not 100% tested in production.

(5) Bias current flows into FB pin. Specification is guaranteed by design and not 100% tested in production.

■ TYPICAL PERFORMANCE CHARACTERISTICS

(T_A=25℃, unless otherwise specified, Test Figure1 above)

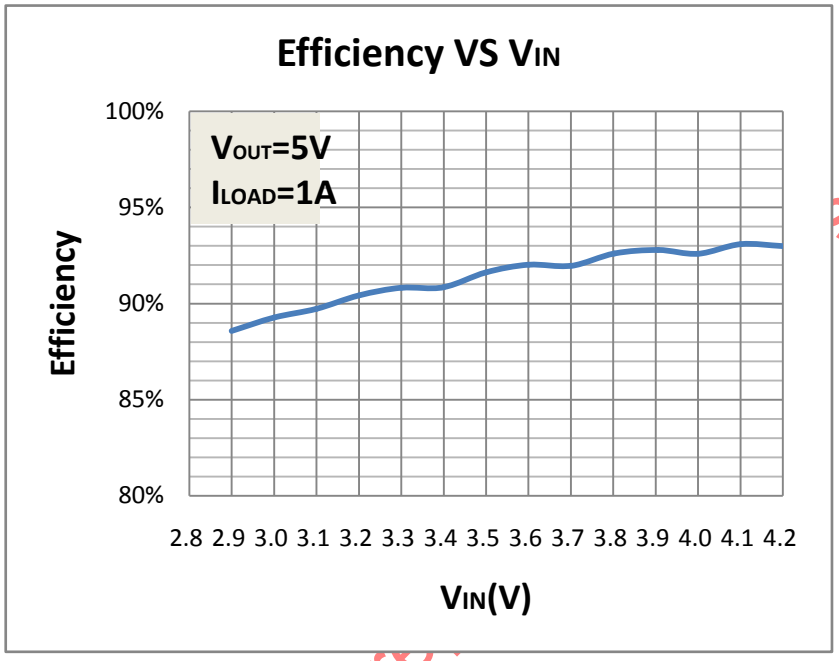


Figure 2

■ BLOCK DIAGRAM

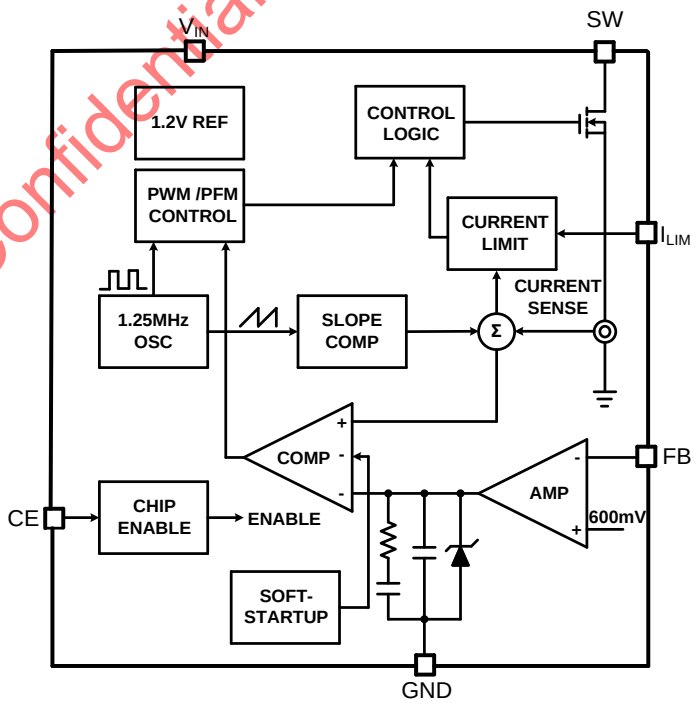


Figure 3

■ DETAILED DESCRIPTION

The CE6373 is a monolithic 1.25MHz boost converter housed in a 6-lead SOT-23 package. The device features current mode PWM control for excellent line and load regulation. The low $R_{DS(ON)}$ NMOS switch enables the device to maintain high efficiency over a wide range of load current. The control loop architecture is peak current mode control. This means that switch duty cycle is directly controlled by the peak switch current rather than only by output voltage.

The CE6373 regulates the output voltage using a combined pulse-width (PWM) and pulse-frequency (PFM) modulation topology. In PWM mode, the device runs at a 1.25MHz fixed frequency. Operation of the feedback loop which sets the peak inductor current to keep the output in regulation can be best understood by referring to the Block Diagram in Figure 3. At the start of each clock cycle a latch in the PWM logic is set and the NMOS switch is turned on. The sum of a voltage proportional to the switch current and a slope compensating voltage ramp is fed to the positive input to the PWM comparator. When this voltage exceeds either a voltage proportional to the 2A current limit or the PWM control voltage, the latch in the PWM logic is reset and NMOS switch is turned off. Slope compensation is necessary to prevent sub-harmonic oscillations that may occur in peak current mode architectures when exceeding 50% duty cycle. The PWM control voltage at the output of the error amplifier is the amplified and compensated difference between the feedback voltage on the FB pin and the internal reference voltage of 0.6V. If the control voltage increases, more current is delivered to the output. When the control voltage exceeds the I_{LIM} reference voltage, the peak current is limited to a minimum of 2A. The current limit helps protect the CE6373 internal switch and external components connected to it. If the control voltage decreases, less current is delivered to the output. During load transients control voltage may decrease to the point where no switching occurs until the feedback voltage drops below the reference. At very light loads, the CE6373 will automatically enter pulse frequency mode (PFM).When the converter output voltage is slightly higher than the preset voltage , the device will stop switching and skip some periods to maintain output regulation.

The CE6373 has an integrated soft-start feature which slowly ramps up the feedback control node from 0V. The soft-start is initiated when CE is pulled high.

Additional features include Cycle-By-Cycle Current Limit Protection, Under Voltage Protection and Over Temperature Protection.

PWM/PFM Auto Switching

The CE6373 offers PWM/PFM automatic switching operation. The PWM operation is shifted to the PFM operation automatically at light load to improve efficiency at light load. So it maintains high efficiency over a wide range of load currents.

Soft Start-Up

Soft start circuitry is integrated into CE6373 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

Cycle by Cycle Current Limit

The CE6373 uses a cycle-by-cycle current limit circuitry to limit the inductor peak current in the event of an overload condition. The current flow through inductor in charging phase is detected by a current sensing circuit. As the value comes across the current limiting threshold the NMOS turns off, so that the inductor will be forced to leave charging stage and enter discharging stage. Therefore, the inductor current will not increase over the current limiting threshold.

Current Limit Program

A resistor between I_{LIM} and GND pin programs peak switch current. The resistor value should be between 19k and 96k. The current limit will be set from 2.5A to 0.5A. Keep traces at this pin as short as possible. Do not put capacitance at this pin.

$$\mathbf{I_{LIM} = \frac{48000}{R_{ILIM}}}$$

UVLO Protection

To avoid malfunction of the CE6373 at low input voltages, an under voltage lockout is included that disables the device, until the input voltage exceeds 2.2V (Typ.).

Over Temperature Protection (OTP)

The CE6373 features integrated thermal overload protection. A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown happens

at a internal junction temperature of 150°C. When the thermal shutdown is triggered, the device automatically turns off the power MOSFET and disables the controller, until the internal junction temperature decreases to typically 30°C below the thermal shutdown trip point. Then the device is released from shutdown automatically and starts switching again.
Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; heating up due to the fault, and then shutting down upon reaching the thermal shutdown point.

Shutdown Mode Operation

Pulling the CE pin low (<0.4V) forces the device in shutdown mode. In shutdown mode, the reference, control circuit, and the main NMOS switch are turned off, drawing <1μA supply current. As with all non-synchronous boost DC/DC converters, the external Schottky diode provides a DC path from the input to the output in shutdown mode. As a result, the output drops to one diode voltage drop below the input in shutdown.
Setting the CE pin high (>1.5V) will turn on the IC again.
For proper operation, the CE pin must be terminated and must not be left floating

■ APPLICATION INFORMATION

Because of the high integration in the CE6373 IC, the application circuit based on this boost converter IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, feedback resistors (R1 and R2) and output rectify diode need to be selected for the targeted application specifications. External component selection for the application circuit depends on the load current requirements. Certain tradeoffs between different performance parameters can also be made. The following sections describe selection of components for a boost converter.

Power Inductor Selection

A 3.3uH inductor is recommended to connect from IN to SW. The minimum and maximum inductor values are constrained by many considerations. The minimum inductance is limited by the peak inductor-current value. The ripple current in the inductor is inversely proportional to the inductance value, so the output voltage may fall out of regulation if the peak inductor current exceeds the current-limit value (2A minimum). Using a nominal 3.3uH inductor allows full recommended current operation even if the inductance is 20% low (2.64 uH) due to component variation.
A maximum 4.7uH (typical) inductor value is recommended to maintain adequate phase margin over the full range of recommended operating conditions.
The saturation current of inductor should be higher enough than the peak switch current. And the inductor should have low core losses at 1.25MHz and low DCR (copper wire resistance).

Output Capacitor Selection

Connect the boost-converter output capacitance from Output to the reference ground plane. The Output capacitance controls the ripple voltage on the Output rail and provides a low-impedance path for the switching and transient-load currents of the boost converter. It also sets the location of the output pole in the control loop of the boost converter. There are limitations to the minimum and maximum capacitance on Output. The recommended minimum capacitors on Output are two 10uF/16V(or one 22uF/16V), X5R or X7R ceramic capacitor. The low ESR of the ceramic capacitor minimizes ripple voltage and power dissipation from the large, pulsating currents of the boost converter and provides adequate phase margin across all recommended operating conditions.

Input Capacitor Selection

Connect the input capacitance from V_{IN} to the reference ground plane. Input capacitance reduces the ac voltage ripple on the input rail by providing a low-impedance path for the switching current of the boost converter. The CE6373 does not have a minimum or maximum input capacitance requirement for operation, but a 22uF/16V, X7R or X5R ceramic capacitor is recommended for most applications for reasonable input-voltage ripple performance. There are several scenarios where it is recommended to use additional input capacitance.

Output Diode Selection

The output rectifier diode supplies current path to the inductor when the internal NMOS is Turned off. Use a schottky diode with low forward voltage to reduce losses. The diode should be rated for a reverse blocking voltage greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor

current. The output rectify diode select requirements are listed as below:

- Low forward voltage
- High switching speed: 50ns max.
- Reverse voltage : V_{OUT} + V_F or more
- Rated current : I_{PK} or more

Programming The Output Voltage

For the CE6373 adjustable output version, the internal 0.6V reference voltage is compared to the voltage at the FB pin to generate an error signal at the output of the error amplifier. The output voltage is set by an external resistive voltage divider from the OUT to FB. The current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network less than 100k is recommended.

Typically, a minimum current of 40μA flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 10kΩ is typically selected. The resistors are then calculated as: $R1=V_{FB}/60\mu A=10k\Omega$, $R2= R1X\ [(V_{OUT}-V_{FB})/V_{FB}]$, $V_{FB}=0.6V$

To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2.

The use of 1% accuracy metal film resistor is recommended for the better output voltage accuracy.

EXAMPLE

During the Application Information section one specific example will be used to define and work with the different equations.

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	3.6	V
Minimum Input Voltage	$V_{IN(min)}$	2.9	V
Output Voltage	V_{OUT}	5.0	V
Input Current Limit set by R_{ILIM}	I_{LIM}	1.6	A
Feedback Voltage	V_{FB}	0.6	V
Switching Frequency	f	1.25	MHz
Estimated Efficiency	η	90	%
Inductor Value of Choice	L1	3.3	μH
Output Capacitor Value of Choice	C_{OUT}	10x 2	μF
Input Capacitor Value of Choice	C_{IN}	22	μF
Output Rectifier Diode V_F of Choice	$V_{F(D1)}$	0.4	V
Feedback Divider Resistor of Choice	R1	13.7	kΩ
	R2	100	kΩ

PCB LAYOUT CONSIDERATION

In the CE6373 boost regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the filter inductor, to the SW pin, to the internal NMOS switch, to the ground and back to the input capacitor, when the switch turns on. The second loop starts from input capacitor, to the filter inductor, to the SW pin to the external output rectifier diode, to the ground and back to the input capacitor, when the switch is off.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and GND pin of the CE6373

A good circuit board layout aids in extracting the most performance from the CE6373. Poor circuit layout degrades the output ripple and the electromagnetic interference (EMI) or electromagnetic compatibility (EMC) performance.

Several layout tips are listed below for the best electric and thermal performance. Figure 4 below illustrates the PCB layout example as reference.

1) Do not use thermal relief connection to the IN and the GND pin. It is desirable to pour a maximized copper area connecting to GND pin and the IN to help thermal dissipation and achieve the best noise performance.

2) If the board space allowed, a ground plane is highly desirable.

3) Use separate analog and power ground planes. Connect the sensitive analog circuitry (such as feedback divider resistors) to analog ground; connect the power components (such as input and output bypass capacitors) to power ground. Connect the two ground planes together near the load to reduce the effects of voltage dropped on circuit board traces.

4) Place the positive terminal of C_{IN} near V_{IN} as closely as possible and the loop area formed by C_{IN} and GND must be minimized to maintain input voltage steady and filter out the pulsing input current. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN} pin, to shunt any high frequency noise to ground.

5) Make the current trace from IN to inductor to SW pin (when internal NMOS turn on) as short as possible to reduce power dissipation and increase overall efficiency. Also the current trace from IN to inductor to output rectifier Schottky diode to C_{OUT} to GND (when internal NMOS turn off) should be as short as possible. Put enough multiply-layer pads when they need to change the trace layer.

6) The GND pin of the IC is the ground connection for high-current power converter node. High current return for the low-side driver and power NMOS. Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors as close as possible, together directly to a power ground plane.

7) The output capacitor, C_{OUT}, should be placed as closely as possible to the negative terminal of the output rectifier Schottky diode and the IC. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple. For additional output voltage filtering, a low ESR ceramic bypass capacitor can be placed in parallel with C_{OUT}, to shunt any high frequency noise to ground. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the output, and the CE6373 GND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the output.

8) The output filter of the boost converter is also critical for layout. The Diode and Output capacitors should be placed to minimize the area of current loop through Output – PGND – SW.

9) The PCB copper area associated with SW、inductor and Schottky diode switching node must be minimized to reduce EMI and voltage overshoot, and avoid the potential noise problem.

10) Avoid routing high impedance traces, such as FB, near the high current traces and components or near the Diode node (D). The feedback network, resistors R1 and R2 must be connected to FB pin directly as closely as possible. And FB is a sensitive signal node, trace area at FB pin should be small. Please keep it away from the inductor, SW、inductor and Schottky diode switching node on the PCB layout to avoid the noise inject into the system.

The feedback networks should be connected directly to a dedicated analog ground plane.

11) If high impedance traces are routed near high current and/or the SW node, place a ground plane shield between the traces.

12) Pour copper plane on all unused board area and connect it to stable DC nodes, like IN, ground or OUT.

13) If the system chip interfacing with the CE pin has a high impedance state at shutdown mode and the IN is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the CE and GND pins to prevent the noise from falsely turning on the boost regulator at shutdown mode.

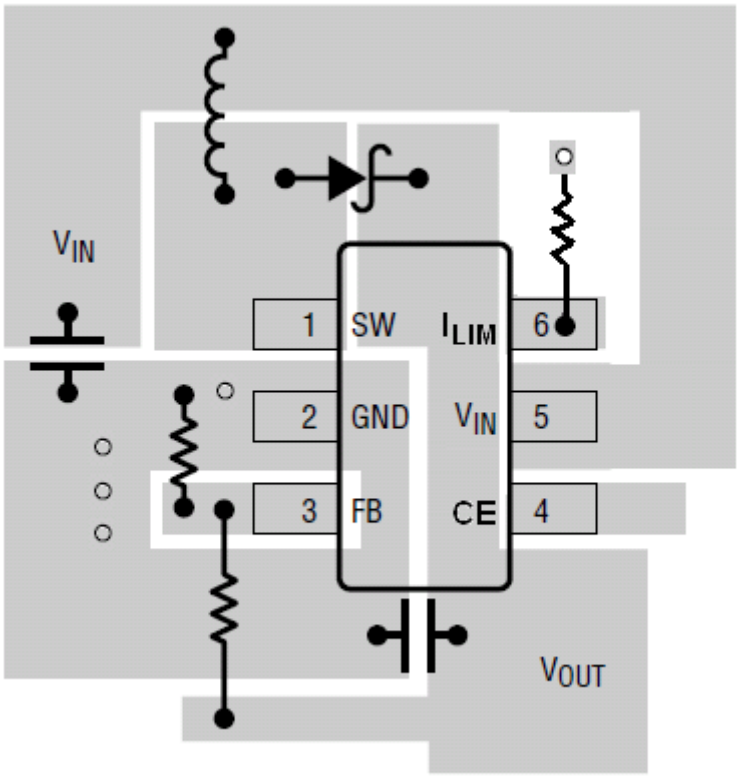
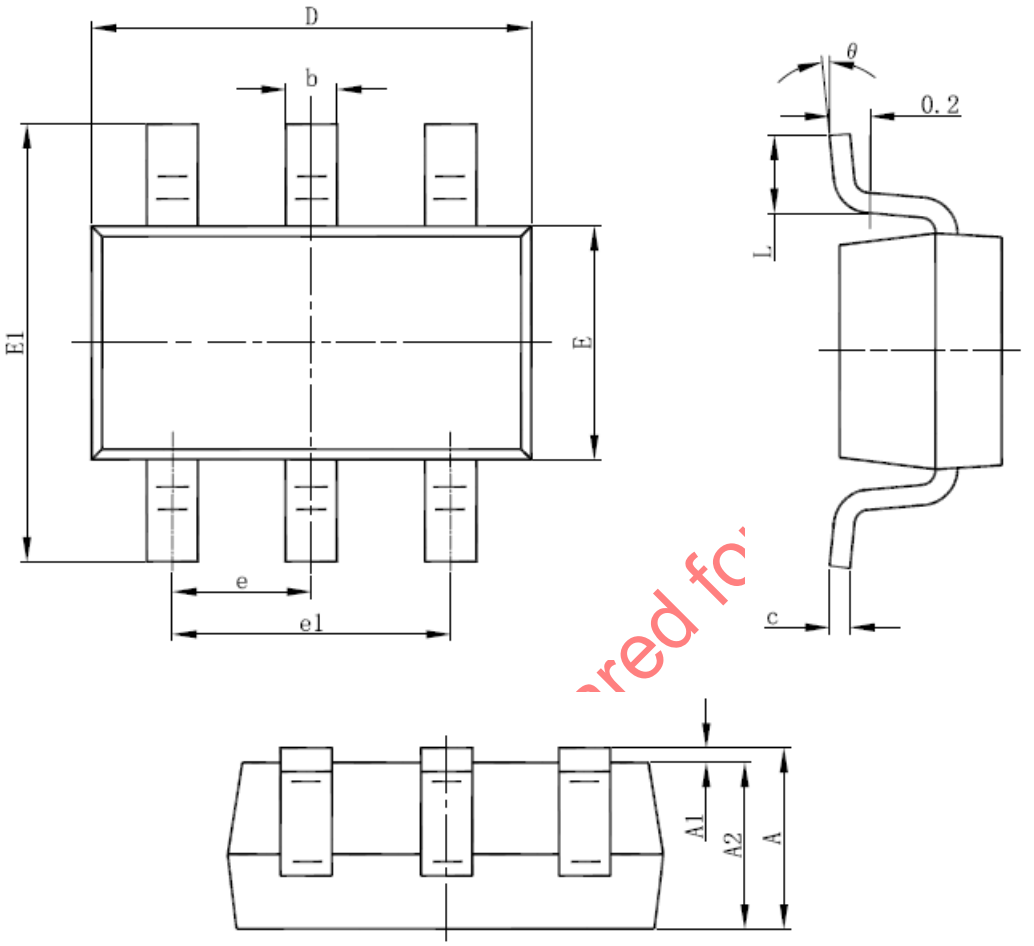


Figure 4. Recommended Top layer Component Placement for two Layers Board

■ PACKAGING INFORMATION

● SOT-23-6 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°