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5A, 500KHz Synchronous Boost Converter with Output Disconnect

CE8421 Series

■ INTRODUCTION:

The CE8421 devices provide a power supply solution for products powered by either a one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline, NiCd or NiMH battery. The converter generates a stable output voltage that is adjusted by an external resistor divider. It provides high efficient power conversion and is capable of delivering output currents up to 2.1A at 5V at a supply voltage down to 3V.

The implemented boost converter is based on a fixed switching frequency (500kHz typical), current-mode controller using a synchronous rectifier to obtain maximum efficiency. Boost switch and rectifier switch are connected internally to provide the lowest leakage inductance and best EMI behavior possible. The current-mode control scheme provides fast transient response and good output voltage accuracy. At light load, the converter will automatically enter into Pulse Frequency Modulation (PFM) operation to reduce the dominant switching losses. During PFM operation, the IC consumes very low quiescent current and maintains high efficiency over a wide load current range.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery.

The device allows use of small inductors and output capacitors for USB devices.

■ FEATURES:

- Up to 90% Efficiency at I_{OUT}=2A V_{OUT}=5V from 3.3V Input
- Low Device Quiescent Current: 70μA (Max)
- Guaranteed 2.5A Output Current at V_{OUT}=5V from 3.3V Input
- 500kHz PWM Switching Frequency
- Synchronous and Embedded Power MOSFETs; No Schottky Diode Required
- Low $R_{DS(ON)}$ (main switch/synchronous switch) at 5.0V output: 35/42mohm
- Input Voltage Range: 1.8V to 5.25V
- Adjustable Output Voltage Range: from 2.5V to 5.5V
- Pulse Frequency Modulation Operation for Improved Efficiency at Low Output Power
- Current Mode Operation with Internal Compensation for Excellent Line and Load Transient Response
- Logic Controlled Shutdown(<1μA)
- Load Disconnect During Shutdown
- Automatic output discharge at shutdown: No output discharge function
- Internal Soft-Start to Limit Inrush Current
- Over Current Protection
- Input Under Voltage Lockout
- Output Over Voltage Protection
- Over-Temperature Protection
- Available in thermally enhanced 8-pin SOP Package

■ APPLICATIONS：

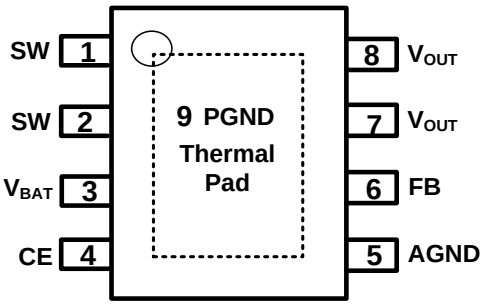
- All Single Cell Li or Dual Cell Battery Operated Products as Tablet PC, Smartbook and Other Portable Equipment
- Products including portable HDMI and USB-OTG
- USB Hosts Without Native 5V Supplies
- USB Charging Port (5V)
- Power Bank, Battery Backup Units
- Wireless Peripherals
- Portable Audio Players
- Personal Medical Devices
- Industrial Metering Equipments
- DC/DC Micro Modules

■ ORDER INFORMATION

Device No.	Output Voltage	Package	Packaging
CE8421AES	Adjustable	SOP8-PP	3000 parts per reel

■ PIN CONFIGURATION:

Top View



SOP8-PP

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1,2	SW	I	**Boost and Rectifying Switch Input**. Connect an inductor between this pin and V_{IN}. Keep the PCB trace lengths as short and wide as is practical to reduce EMI and voltage overshoot. If the inductor current falls to zero, or pin CE is low, an internal anti-ringing switch is connected from this pin to V_{IN} to minimize EMI.
3	V_{BAT}	I	**Battery Supply Input Voltage**. The device gets its start-up bias from V_{BAT}. Once V_{OUT} exceeds 2.3V, bias comes from V_{OUT}. Thus, once started, operation is completely independent from V_{BAT}. Operation is only limited by the output power level and the battery's internal series resistance. The V_{BAT} pin should be connected to the positive terminal of the battery and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{BAT} pin, and the CE8421 PGND pin. The minimum recommended bypass capacitance is 1μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{BAT} pin and the PGND pin. PCB trace length from V_{BAT} to the input filter capacitor(s) should be as short and wide as possible.
4	CE	I	**Chip Enable Input**. Internal integrated with 1Mohm pull down resistor. CE=High: Normal free running operation. CE=Low: Shutdown; quiescent current <1μA. Output capacitor can be completely discharged through the load or feedback resistors. If CE is undefined, pin SW may ring.

5	AGND	I	**Analog Ground.** The analog ground ties to all of the noise sensitive signals. Provide a clean ground for the analog control circuitry and should not be in the path of large currents. Return for output voltage set resistor divider. Connect this pin to PGND.
6	FB	I	**Feedback Input**. Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 2.5V to 5.5V by: V_{OUT} =1.2V•[1+(R1/R2)] The feedback networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the AGND pin. If no analog ground plane is available, then the ground connection of the feedback network must tie directly to the AGND pin. Connecting the network to the PGND can inject noise into the system and effect performance. The feedback network, resistors R1 and R2 must be connected to FB pin directly as closely as possible. And FB is a sensitive signal node, trace area at FB pin should be small. Please keep FB away from the inductor and SW switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
7,8	V_{OUT}	O	**DC-DC Power Output, IC Supply Voltage and Output Voltage Sense Input** (Drain of the Internal Synchronous Rectifier P-MOSFET). PCB trace length from V_{OUT} to the output filter capacitor(s) should be as short and wide as possible. Care should be taken to minimize the loop area formed by the output filter capacitor(s) connections, the V_{OUT} pin, and the CE8421 PGND pin. The minimum recommended output filter capacitance is 22μFx2 ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the PGND pin. V_{OUT} is completely disconnected from V_{BAT} when CE is low, due to the output disconnect feature. Bias is derived from V_{OUT} when V_{OUT} exceeds 2.3V.
9	PGND	P	**Power Ground.** Ground connection for high-current power converter node. High current return for the low-side driver and power main switch N-MOSFET. Connect PGND with large copper areas directly to the input and output supply returns and negative terminals of the input and output filter capacitor(s). Tie this pin to the ground island/plane through the lowest impedance connection available. Connect this pin to AGND.

(1) I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER		SYMBOL	RATINGS	UNITS
CE Voltage(2)		V_{CE}	V_{OUT}+0.3	V
Other Pins Voltage(2)			6	V
Power Dissipation(3)	SOP8-PP	P_D@T_A=25°C	1	W
Package Thermal Resistance(4)		θ_{JA}	125	°C/W
Operating Junction Temperature Range		T_j	150	°C
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	°C
Storage Temperature Range		T_{stg}	-65~150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = [T_J(MAX)-T_A]/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

(4) θ_{JA} is measured in the natural convection at T_A=25℃ on a two-layer Chipower Evaluation Board

■ RECOMMENDED OPERATING CONDITIONS(5)

	MIN	NOM	MAX	UNITS
Supply voltage at V_{BAT}	1.8		5.25	V
Output voltage at V_{OUT}	2.5		5.5	V
CE	0		V_{OUT}+0.3	V
All other pins	0		5.5	V
Operating Ambient temperature range, T_A	-40		85	°C
Operating junction temperature range, T_j	-40		125	°C

(5) The device is not guaranteed to function outside its operating conditions.

■ ELECTRICAL CHARACTERISTICS

(V_{CE}=V_{BAT}=3.6V, V_{OUT}=5V, L=1.5μH, C_{IN} = 47μF, C_{OUT} = 68μF, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP[6]	MAX	UNITS
Input V_{IN} UVLO Threshold	V_{UVLO}	V_{IN} Rising			1.78	V
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}			0.1		V
Input Quiescent Current	I_{BAT}	V_{BAT}=3.6V, V_{FB}=1.28V, No load, no switching (exclude input current from CE)		50	70	μA
Shutdown Current	I_{SHDN}	V_{CE}=0V		0.1	1	μA
CE High-Level Threshold	V_{CEH}	CE Rising	1.2			V
CE Low-Level Threshold	V_{CEL}	CE Falling			0.4	V
Soft-start time	T_{SS}			3		ms
Feedback Reference Voltage	V_{FB}		1.182	1.2	1.218	V
Output Over Voltage Protection	V_{OVP}			5.7		V
Low Side Main N-FET R_{ON} [7]	$R_{NDS(ON)}$	V_{OUT}=5V		35	55	mΩ
Synchronous P-FET R_{ON} [7]	$R_{PDS(ON)}$	V_{OUT}=5V		42	60	mΩ
Switching Frequency	F_{SW}			500		KHz
Maximum Duty Cycle	D_{MAX}		90	95	97	%
Main N-FET Current Limit[8] [9]	I_{LIM1}		5.0	6.2		A
Thermal Shutdown[7]	T_{SD}			150		°C
Thermal Shutdown Hysteresis[8]	T_{HYS}			20		°C

(6) Typical numbers are at 25℃ and represent the most likely norm.
(7) Does not include the bond wires. Measured directly at the die.
(8) Specification is guaranteed by characterization and not 100% tested in production.
(9) Duty cycle affects current limit due to ramp generator.

■ TYPICAL APPLICATION CIRCUIT

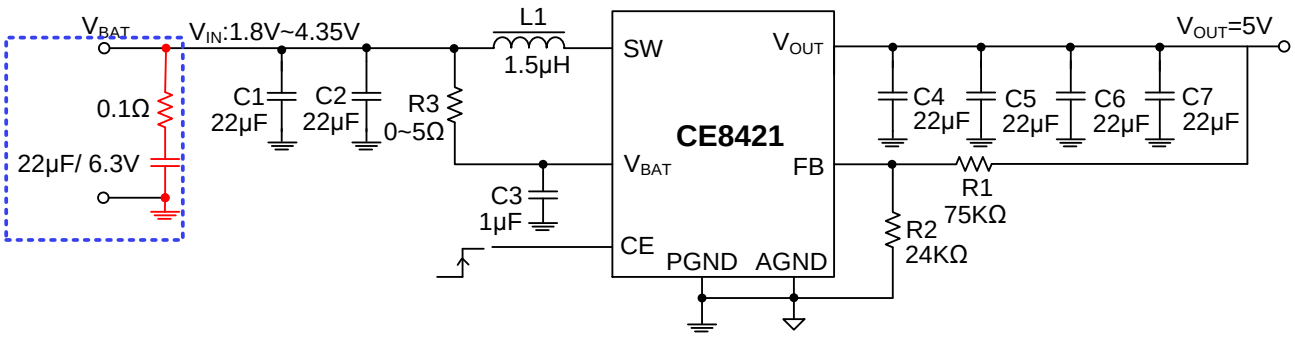


Figure 1 Standard Application Circuit

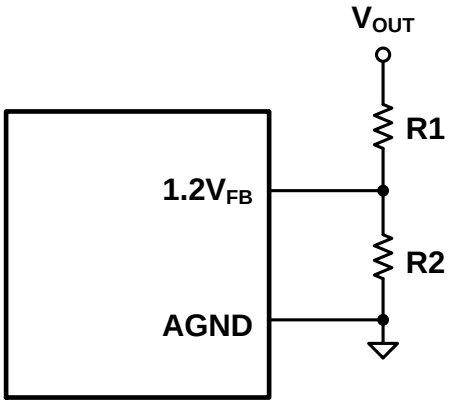
■ APPLICATION INFORMATION

PROGRAMMING THE OUTPUT VOLTAGE

The CE8421 internal 1.2V reference voltage is compared to the voltage at the FB pin to generate an error signal at the output of the error amplifier. The output voltage is set by an external resistive voltage divider from the V_{OUT} to FB. The current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network less than 100k is recommended.

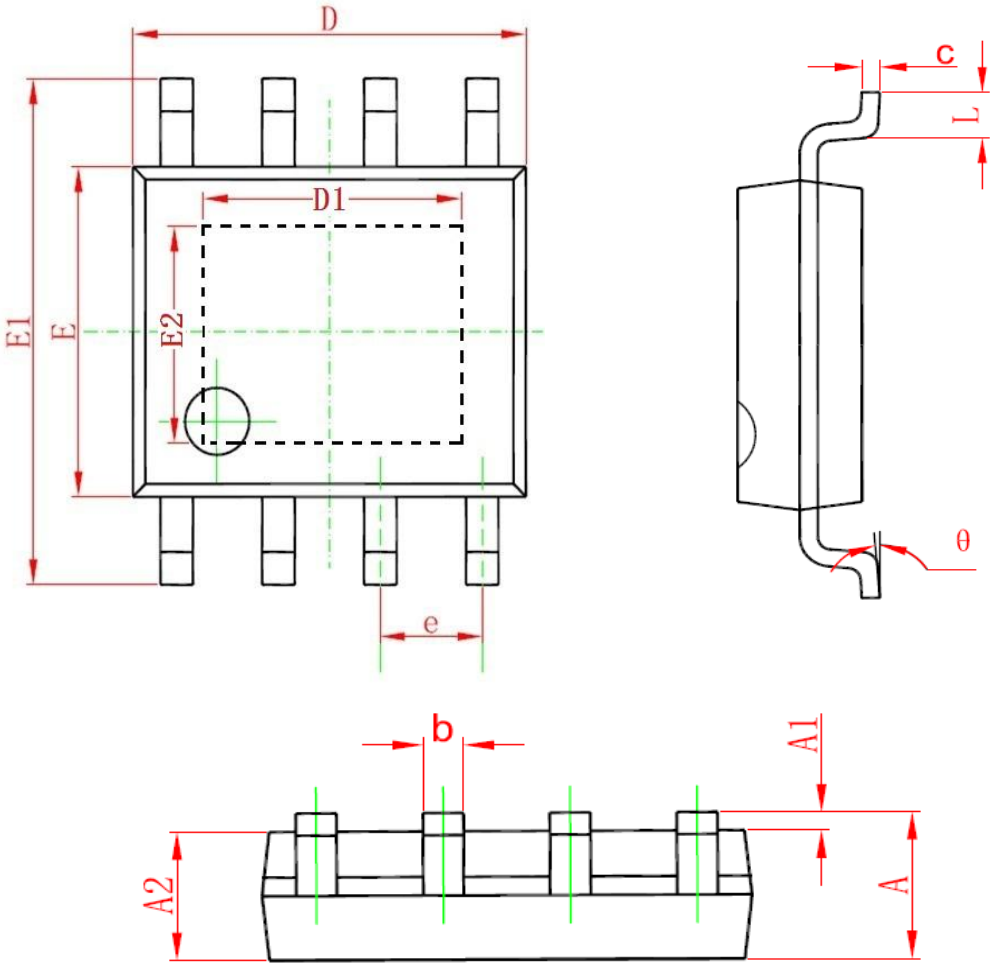
Typically, a minimum current of 40μA flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 24kΩ is typically selected. The resistors are then calculated as: $R2=V_{FB}/50\mu A=24k\Omega$, $R1= R2X\ [(V_{OUT}-V_{FB})/V_{FB}]$, $V_{FB}=1.2V$

The use of 1% accuracy metal film resistor is recommended for the better output voltage accuracy.



■ PACKAGING INFORMATION

● SOP8-PP Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0. 250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.100	3.500	0.122	0.137
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.200	2.600	0.086	0.102
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°