Applications Note:CE8442

High Efficiency 1MHz, 2A Step Up Regulator

Preliminary Specification

General Description

The CE8442 is a high efficiency boost regulator targeted for general step-up applications.

Ordering Information

CE8442 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
CE8442ABC	SOT23-6	2A

Features

- Wide input range: 3-8V bias input, 16Vout max
- 1MHz switching frequency
- Minimum on time: 100ns typical
- Minimum off time: 100ns typical
- Low $R_{DS(ON)}$: 150mΩ
- RoHS Compliant and Halogen Free
- Accurate Reference: 0.6V_{REF}
- Compact package: SOT23-6

Applications

- WLED Drivers
- Networking cards powered from PCI or PCI-express slots

Typical Applications

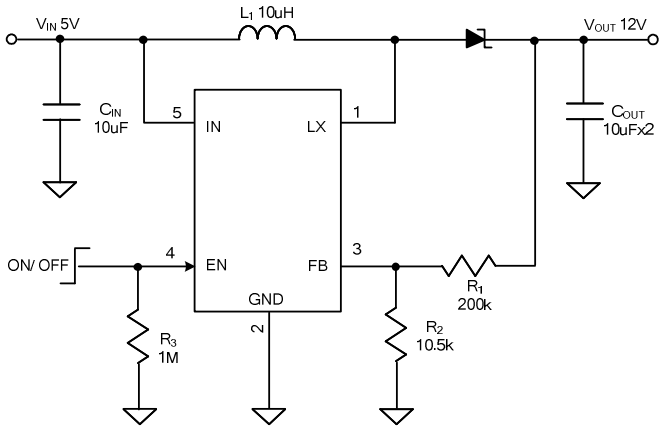


Figure 1. Schematic Diagram

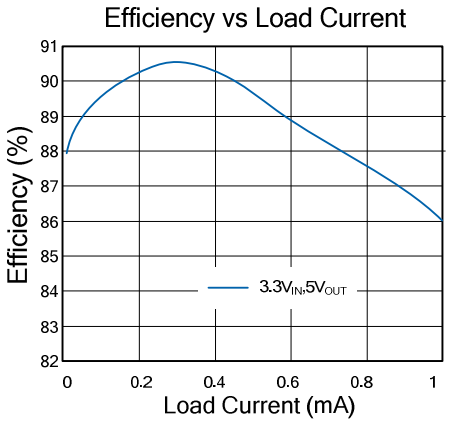
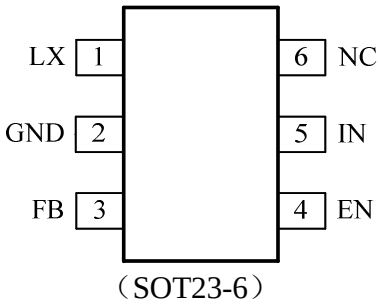


Figure 2. Efficiency vs Load Current

Pinout (top view)



（SOT23-6）

Top Mark: LE*xyz* **(**Device code: LE, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
IN	5	Input pin. Decouple this pin to GND pin with 1uF ceramic cap.
GND	2	Ground pin
LX	1	Inductor node. Connect an inductor between IN pin and LX pin.
FB	3	Feedback pin. Connect a resistor R1 between V_{OUT} and FB, and a resistor R2 between FB and GND to program the output voltage: V_{OUT}=0.6V*(R1/R2+1).
EN	4	Enable control. High to turn on the part. Don't leave it floated.
NC	6	No connection.

Absolute Maximum Ratings (Note 1)

LX, IN, EN ---------- 18V
All other pins---------- ---------- 3.6V
Power Dissipation, P_D @ T_A = 25°C SOT23-6 ---------- 0.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 161°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Input Voltage Supply---------- 3V to 8V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		8	V
Quiescent Current	I_Q	V_{FB}=0.66V		100		μA
Shutdown Current	I_{SHDN}	EN=0			15	μA
Low Side Main FET RON	Rds(on)			150		mΩ
Main FET Current Limit	I_{LIM1}		2			A
Switching Frequency	Fsw		0.8	1	1.2	MHz
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$				1.8	V
UVLO Hysteresis	$U_{VLO,HYS}$			0.1		V
Thermal Shutdown Temperature	T_{SD}			150		°C
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
EN Pin Input Current	I_{EN}		0		100	nA
Max Duty Cycle				90		%

Note 1: Stresses listed beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may remain possibility to affect device reliability.

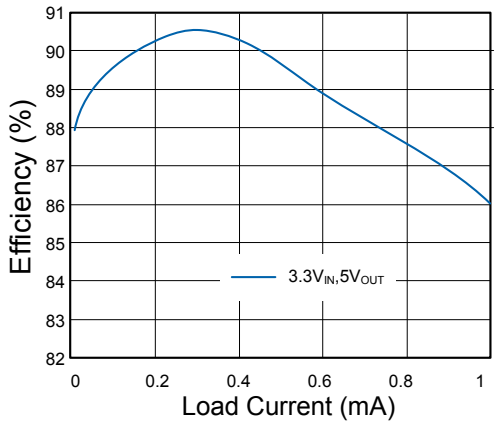
Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: IC could be start up in 1.8V.

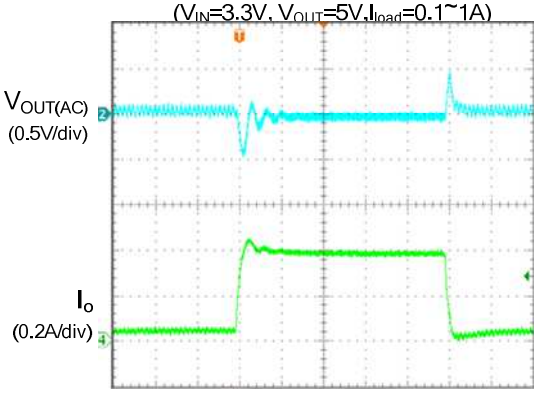
Typical Performance Characteristics

Efficiency vs Load Current



Load Transient

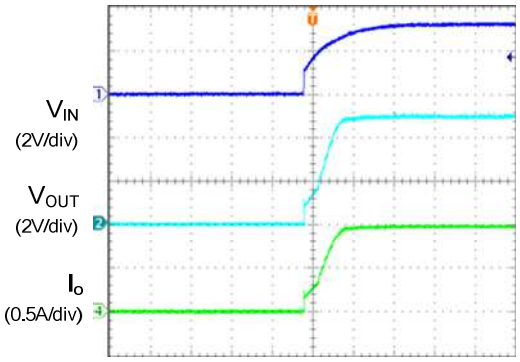
(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=0.1~1A)



Time(100us/div)

Startup from V_{IN}

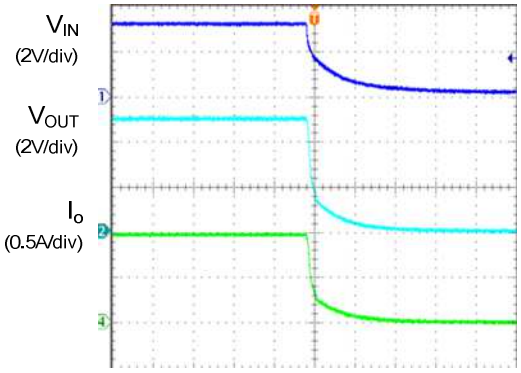
(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1A)



Time(4ms/div)

Shutdown from V_{IN}

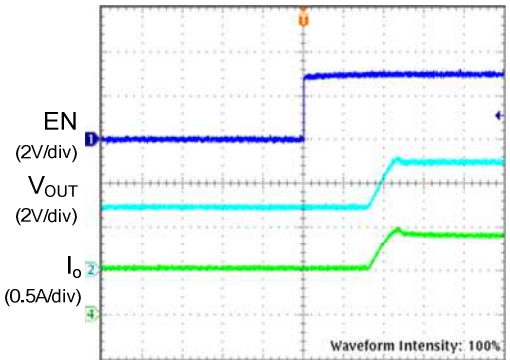
(V_{IN}=3V, V_{OUT}=5V,I_{load}=1A)



Time(2ms/div)

Startup from Enable

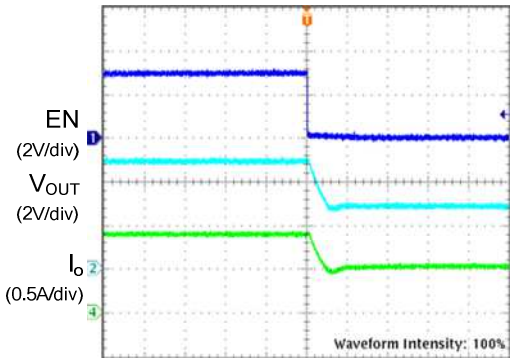
(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1A)



Time(100us/div)

Shutdown from Enable

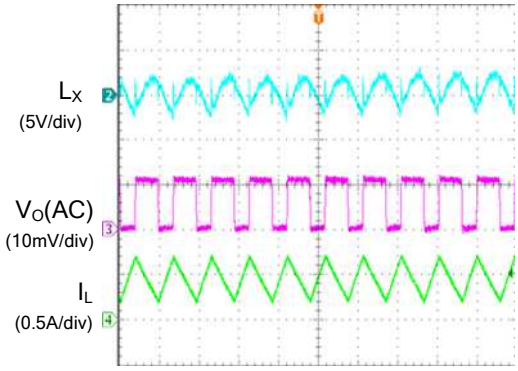
(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1A)



Time(100us/div)

Output Ripple

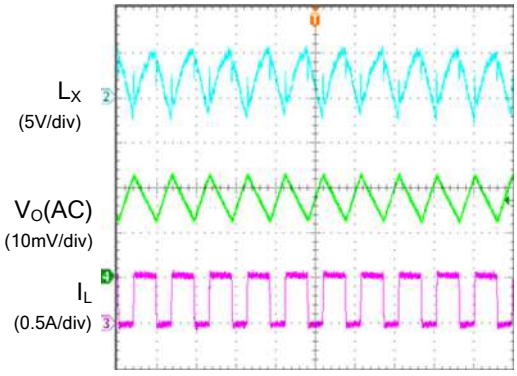
(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=300mA)



Time(1us/div)

Output Ripple

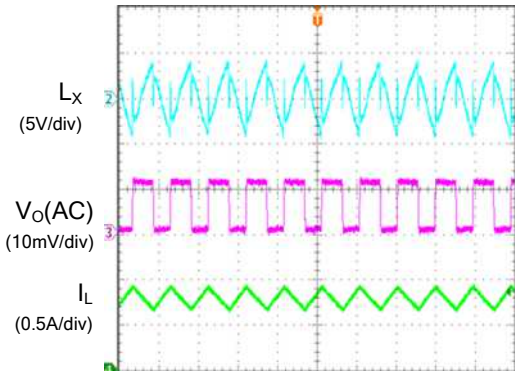
(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=500mA)



Time(1us/div)

Output Ripple

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1A)



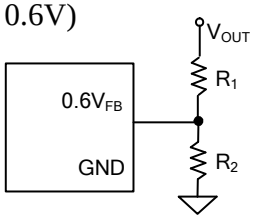
Time(1us/div)

Applications Information

Because of the high integration in the CE8442 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2:
Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = (R_1 \times 0.6V)/(V_{OUT} - 0.6V)$$



Input capacitor C_{IN}:
The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.In this case a 10uF low ESR ceramic is recommended.

Output capacitor C_{OUT}:
The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 25V rating and more than two pcs 10uF capacitor.

Boost inductor L:
There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,\,MAX} \times 40\%}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The CE8442 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT\_MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Enable Operation
Pulling the EN pin low (<0.4V) will shut down the device. During the shut down mode, the CE8442 shut down current drops to lower than 1uA, Driving the EN pin high (>1.5V) will turn on the IC again.

Soft-start(En Control)
The CE8442 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. 200us turn on delay time before the initial soft-start, the typical soft-start time is 1ms.

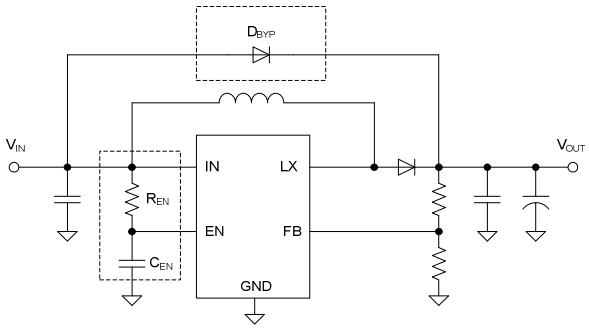
Diode Selection
Schottky diode is a good choice for high efficiency operation because of its low forward voltage drop and fast reverse recovery. The current rating of the diode must meet following:

$$I_D(RMS) \approx \sqrt{(I_{OUT} \times I_{PEAK})}$$

The schottky diode reverse breakdown voltage should be larger than the output voltage.

Applications with Large Bulk Capacitance

In applications with large bulk capacitance on the output, a very high inrush current can be seen flow through the inductor during power on. To avoid this inrush current flow into the IC and cause any unexpected damage, a Zener diode connected from power input to the output or an RC delay circuit added on EN pin of the IC can be used. Refer to the circuit below.



Layout Design:

The layout design of CE8442 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

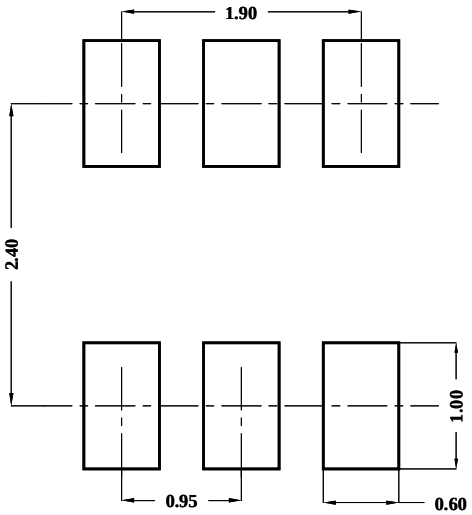
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

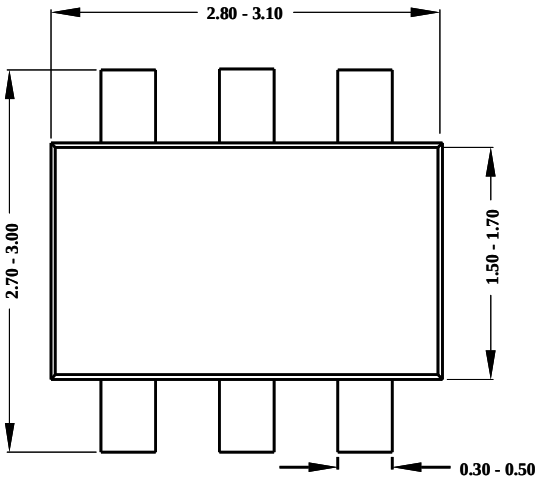
4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

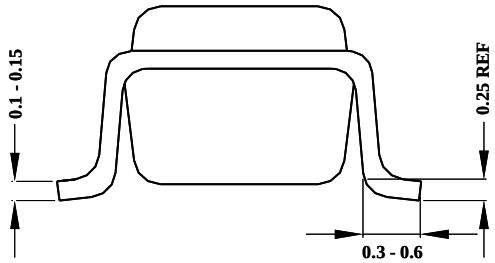
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

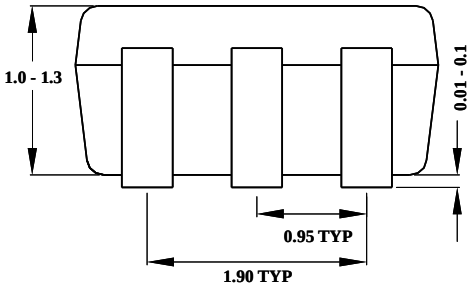
SOT23-6 Package outline & PCB layout design



Recommended Pad Layout



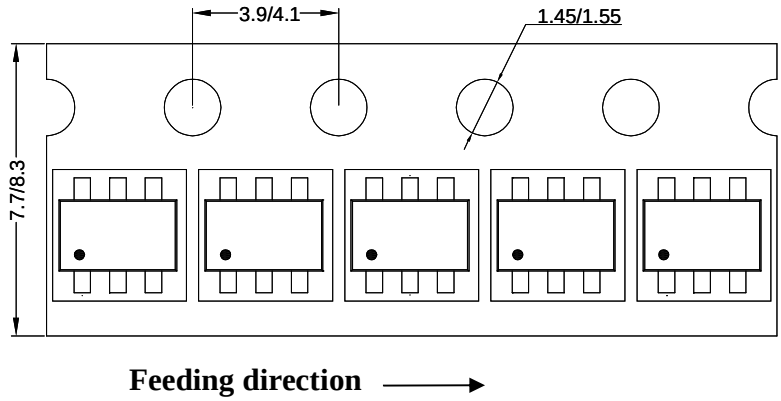




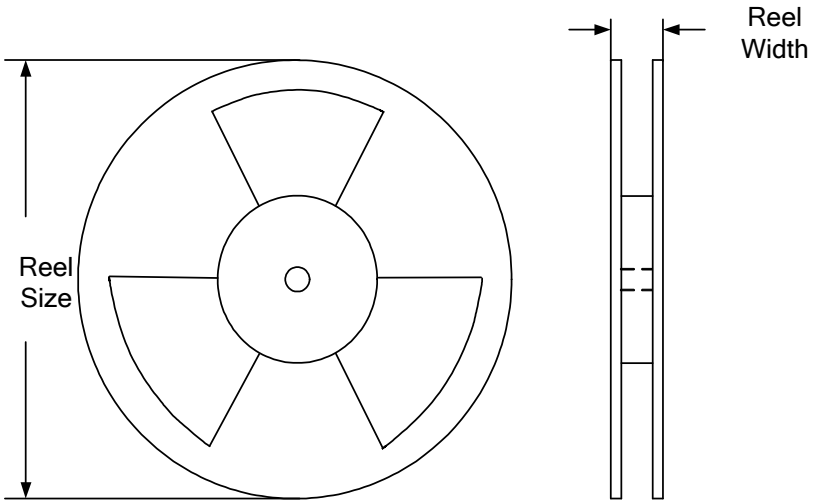
Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

1. SOT23-6 (SOT26)



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	8.4	280	160	3000

3. Others: NA